ABSTRACTED-PUB-NO:DE 4023981A
BASIC-ABSTRACT:The LCD has x-axis and y-axis drivers (112,114), an LCD screen (116) and a serial-parallel converter (110). The latter converts serial analogue image data into parallel analogue image data and can operate at high speed. The x-axis driver, which can operate at low speed, receives parallel analogue image data and delivers it for a horizontal display line of the LCD. The analogue display data are extracted cyclically from the converter using a latch clock. ADVANTAGE - Has multiple shade control and can display not fewer than nine colours using analogue input.

ABSTRACTED-PUB-NO:DE 4023981C
EQUIVALENT-ABSTRACT:The liquid-crystal display control method involves converting the digital indicating data (117R, 117G, 117B) for each pixel, which possess a breadth of several bits corresponding to the brightness, into analogue indicating data (109R, 109G, 109B) with a voltage value corresponding to the brightness involved. The D/A converter (118) is used for the conversion process. The serial analogue indicating data is converted into parallel analogue indicating data (111R, 111G, 111B) in a serial/parallel converter (110), the latter data having a lower processing speed. The voltage values are supplied by an analogue driving unit (112) for the X axis to a cell of the liquid crystal after the analogue indicating data for a horizontal line has been produced by a sequential transfer of the parallel analogue indicating data. The brightness of each pixel of the liquid-crystal screen (116) is controlled by the two converters mentioned and by the analogue driving unit. ADVANTAGE - Using analogue input signal many colours or intermediate tones can be displayed, not less than nine. A liquid crystal display device for providing signals for application to a liquid crystal display panel having a plurality of display panel rows, to cause a display made up of a plurality of display line, each display panel row of said display panel including a plurality of switching elements, each switching element normally assuming a non-selected state and responsive to application thereto of a selecting voltage for assuming a selected state, each switching element in its selected state applying to an associated display area of the display panel a voltage corresponding to data to be displayed in the associated display area and in its non-selected state retaining the associated display area at its most recent correspondi ng voltage, said liquid crystal display device comprising: a input buffer storage circuit, including a plurality m of first buffer elements, for receiving serial analog display data corresponding to a plurality of display lines and sequentially storing the received display data in said first buffer storage elements; an input holding circuit coupled to said input buffer storage circuit, for receiving and simultaneously holding the plurality of display data stored in said input buffer storage circuit; an output buffer storage circuit, including a plurality n of second buffer storage elements, where n is greater than m, for sequentially receiving said display data held in said input holding circuit and storing the received display data in the second buffer storage elements; and an output holding circuit coupled to said output buffer storage circuit, for receiving and simultaneously holding the display data stored in said output buffer storage circuit and for outputting held display data for application to switching elements of the display panel. An information processor for displaying images, said information processor comprising: (a) a display data memory circuit for storing display information for over one display image as digital data; (b) a readout circuit for successively reading out digital display image data from said display data memory circuit and for producing a timing signal synchronized with the read display data; (c) an analog display data producing circuit, including a converting circuit for successively converting the read out digital display image data to analog display data and outputting said analog display data; (d) an analog display data driving circuit including, a first holding circuit for successively receiving and holding the analog display data, a first output circuit for outputting the analog display data held by said first holding circuit, a second holding

circuit for successively receiving and holding the analog display data outputted by said first output circuit, and a second output circuit for outputting the analog display data held by said second holding circuit; (e) a Y axis direction driving circuit for outputting a selection voltage to successively select horizontal display lines in accordance with the timing signal produced by said readout circuit; and (f) a liquid crystal panel including an X axis direction driving electrode for transmitting the analog display data outputted by said analog display data driving circuit, a Y axis direction driving electrode for transmitting the selection voltage outputted by said Y axis direction driving circuit, a pixel part constituted by switching elements, pixel electrodes and liquid crystal at a location at which the X axis direction driving electrode is crossed by the Y axis direction driving electrode in a matrix state.

CHOSEN-DRAWING:Dwg.5/10 Dwg.5/10 Dwg.7,8/10 Dwg.5/10

TITLE-TERMS:
LCD REPRODUCE NINE COLOUR ANALOGUE INPUT AXIS DRIVE SERIAL PARALLEL CONVERTER CYCLIC DATA EXTRACT

DERWENT-CLASS: P81 P85 T01 T04 U14

EPI-CODES: T01-C04B; T01-C09; T04-H03B; U14-K01A3;
Non-CPI Secondary Accession Numbers:N1991-035335

Term	Documents
#110 and #15	1

DE 3854562G	N/A	1988EP-0108541	May 27, 1988
DE 3854562G	Based on	EP 298243	N/A

IPC: G06F003/15; G09G001/16 ; H04N001/38

ABSTRACTED-PUB-NO:EP 298243A
BASIC-ABSTRACT:The demultiplexer device combines several low-resolution video signals into one of high resolution. The frames from the low resolution signals are stored and read out at a higher rate, so that a number of them are combined side by side and one above the other to give one in which each of the original frames forms a part. Pref. four low-resolution frames are used with a horizontal line, of twice the original pixels, formed by corresponding original pairs of lines. Similarly the two pairs of frames placed one above the other doubles the vertical resolution. The non-data part of each transmission is used to transmit address codes so that a variety of devices can use the same input frames in different ways. USE/ADVANTAGE - Computer video output. Gives higher resolution without higher refreshing bandwidth.

ABSTRACTED-PUB-NO:EP 298243B
EQUIVALENT-ABSTRACT:A system for generating high horizontal resolution video output frames having a plurality of horizontal lines from low resolution video input frames having a plurality of horizontal lines, comprising: means (10) for receiving video input data representing a plurality of low resolution video input frames; means (16) for storing said plurality of low resolution video input frames at a first clock rate; means (18,14) for combining corresponding lines of selected ones of said plurality of stored frames to form a single horizontal line; and means (18) for outputting each said formed single horizontal line at a second clock rate substantially greater than said first clock rate thereby generating a horizontal line output having a higher resolution that the horizontal lines of said low resolution input frames. The generator comprises a device for receiving video input data representing a number of low resolution video input frames and a memory for storing the low resolution video input frames at a first clock rate. Corresp. lines of selected ones of the stored frames are combined to form a single horizontal line. Each of the formed single horizontal line is outputted at a second clock rate greater than the first clock rate thereby generating a horizontal line output having a higher resolution than the horizontal lines of the low resolution input frames. (26pp)

CHOSEN-DRAWING:Dwg.1/11 Dwg.1/11

TITLE-TERMS:
COMPUTER VIDEO DE MULTIPLEX HIGH RESOLUTION PICTURE LOW RESOLUTION FRAME COMBINATION HIGH RESOLUTION STACK READ HIGH RATE

DERWENT-CLASS: P85 T04

EPI-CODES: T04-H01A;
Non-CPI Secondary Accession Numbers:N1989-007162

Full | Citation | Review | Classification | Date | Reference

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2. Document ID: EP 629085 A2 CA 2125334 A JP 07075112 A EP 629085 A3 US 5477397 A,

Relevance Rank: 95

Entry 9 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1995-016036

DERWENT-WEEK: 199606

TITLE:
Digital high-definition television receiver facilitating trick-play modes on digital VCR - decodes received HDTV signal to produce data representing low resolution image, data representing both high and low resolution images being provided by TV receiver at output port

INVENTOR:KIM, H; NAIMPALLY, S V

PATENT-ASSIGNEE: MATSUSHITA ELEC IND CO LTD[MATU], MATSUSHITA DENKI SANGYO KK[MATU], MATSUSHITA ELEC CORP AMERICA[MATU]

PRIORITY-DATA: 1993US-0073789 (June 8, 1993) , 1993US-0021248 (February 23, 1993)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
EP 629085 A2	December 14, 1994	E	019	H04N 005/92
CA 2125334 A	December 9, 1994	N/A	000	H04N 007/12
JP 07075112 A	March 17, 1995	N/A	018	H04N 007/32
EP 629085 A3	April 12, 1995	N/A	000	H04N 005/92
US 5477397 A	December 19, 1995	N/A	017	H04N 005/78

DESIGNATED-STATES: DE FR GB NL

CITED-DOCUMENTS: No-SR.Pub; 2.Jnl.Ref ; EP 541313 ; EP 542196

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
EP 629085A2	N/A	1994EP-0108312	May 30, 1994
CA 2125334A	N/A	1994CA-2125334	June 7, 1994
JP07075112A	N/A	1994JP-0126586	June 8, 1994
EP 629085A3	N/A	1994EP-0108312	May 30, 1994
US 5477397A	CIP of	1993US-0021248	February 23, 1993
US 5477397A	N/A	1993US-0073789	June 8, 1993

IPC: H04N005/78; H04N005/92 ; H04N007/01 ; H04N007/12 ; H04N007/32

RELATED-ACC-NO: 1994-266310

ABSTRACTED-PUB-NO:EP 629085A
BASIC-ABSTRACT:The HDTV receiver comprises a receiver for the encoded high definition video signal, and a decoder (112) for decoding the video signal to produce a decoded digital signal representing the high definition video image. A decimating circuit, responsive to the decoded digital signal, decreases the number of samples in the decoded digital signal to produce a decimated video signal representing a video image having a reduced number of picture elements. An encoder encodes the decimated video signal, using intra-frame encoding techniques to the relative exclusion of predictive encoding techniques, to produce an encoded low resolution video signal. An output circuit provides both the encoded high definition video signal and the encoded low resolution video signal. The low resolution image data is also used by the TV receiver to produce a picture-in -picture (PIP) display.
ADVANTAGE - Uses single high definition television decoder to produce low resolution image data and to produce high resolution video display of television receiver.

ABSTRACTED-PUB-NO:US 5477397A
EQUIVALENT-ABSTRACT:A high-definition television receiver capable of decoding a high-definitio n video signal that was encoded using both

intra-frame and predictive encoding techniques comprising: means for receiving the encoded high-definition video signal; decoding means for decoding the encoded high-definition video signal to produce a decoded digital signal representing a high-definition video image; decimating means, responsive to the decoded digital signal, for decreasing the number of samples in the decoded digital signal to produce a decimated video signal representing a video image having a reduced number of picture elements; means for encoding the decimated video signal, using intra-frame encoding techniques to the relative exclusion of predictive encoding techniques, to produce an encoded low-resolution video signal which is independent of the encoded high-definition video signal; and output means for providing both the encoded high-definition video signal and the encoded low-resolution video signal.

CHOSEN-DRAWING:Dwg.1/10 Dwg.1/10

TITLE-TERMS:
DIGITAL HIGH DEFINE TELEVISION RECEIVE FACILITATE TRICK PLAY MODE DIGITAL VCR DECODE RECEIVE HDTV SIGNAL PRODUCE DATA REPRESENT LOW RESOLUTION IMAGE DATA REPRESENT HIGH LOW RESOLUTION IMAGE TELEVISION RECEIVE OUTPUT PORT

DERWENT-CLASS: W03 W04

EPI-CODES: W03-A11D; W03-A11X; W04-B10B; W04-B10G; W04-F01H5;
Non-CPI Secondary Accession Numbers:N1995-012665

Full | Citation | Review | Classification | Date | Reference

3. Document ID: US 5065346 A,

Relevance Rank: 93

Entry 5 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1991-353380

DERWENT-WEEK: 199148

TITLE:
Low to high resolution display conversion system - uses buffer memory to allow low resolution video data to be simultaneously displayed in window fashion with high resolution video data

INVENTOR:KAWAI, T; TOBISHIMA, T

PATENT-ASSIGNEE: SONY CORP[SONY]

PRIORITY-DATA: 1986JP-0301051 (December 17, 1986)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 5065346 A	November 12, 1991	N/A	000	N/A

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
US 5065346A	N/A	1987US-0128069	December 3, 1987

IPC: G06F003/15; G09G001/16

ABSTRACTED-PUB-NO:US 5065346A
BASIC-ABSTRACT:The low resolution to high resolution display system is arranged such that a low resolution video signal from a personal computer is written in a memory plane in response to an address based on a clock signal produced from the personal computer side. A switching circuit is provided in a video signal path of a high resolution display appts. for switching between the memory plane and the video signal produced by the high resolution display appts. The memory plane is read by an address based on the clock signal of the display appts. produced during a display window period. The video signal read from the memory plane is supplied through the switching circuit to the video signal path of the display appts. USE - For displaying personal computer display signal on high resolution CAD/CAM appts.

CHOSEN-DRAWING:Dwg.1/3

TITLE-TERMS:
LOW HIGH RESOLUTION DISPLAY CONVERT SYSTEM BUFFER MEMORY ALLOW LOW RESOLUTION VIDEO DATA SIMULTANEOUS DISPLAY WINDOW FASHION HIGH RESOLUTION VIDEO DATA

DERWENT-CLASS: P85 T01 T04

EPI-CODES: T01-C04A; T01-J15; T04-H01;
Non-CPI Secondary Accession Numbers:N1991-270698

Full | Citation | Review | Classification | Date | Reference

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4. Document ID: JP 07107441 A,

Relevance Rank: 93

Entry 10 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1995-202642

DERWENT-WEEK: 199527

TITLE:
Video signal transmitting and receiving device - incorporates multiplexing circuit at transmission side which multiplexes data packets corresponding to compressed low resolution video signal

PATENT-ASSIGNEE: TOSHIBA KK[TOKE]

PRIORITY-DATA: 1993JP-0244867 (September 30, 1993)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 07107441 A	April 21, 1995	N/A	013	H04N 007/00

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP07107441A	N/A	1993JP-0244867	September 30, 1993

IPC: H04N007/24

ABSTRACTED-PUB-NO:JP07107441A
BASIC-ABSTRACT:The video signal transmitting and receiving device incorporates multiple encoding circuits (610-614) which encodes number of low resolution video signals. The compressed video signals from the encoding circuits is sent as data packets from multiple circuits (615-619) corresponding to N channels are multiplexed in a multiplexing circuit (620). This multiplexed video data is transmitted through a channel with high degree of resolution. In the reception side, a demultiplexing circuit (650) selects the signals for requisite channel for processing. The requisite signal is selected by recognising the header part of data packets using a decoder unit (640). ADVANTAGE - Increases freedom of selection of channels at reception side.

CHOSEN-DRAWING:Dwg.1/12

TITLE-TERMS:
VIDEO SIGNAL TRANSMIT RECEIVE DEVICE INCORPORATE MULTIPLEX CIRCUIT TRANSMISSION SIDE MULTIPLEX DATA PACKET CORRESPOND COMPRESS LOW RESOLUTION VIDEO SIGNAL

DERWENT-CLASS: W02

EPI-CODES: W02-F08; W02-K03;
Non-CPI Secondary Accession Numbers:N1995-159248

Full | Citation | Review | Classification | Date | Reference

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5. Document ID: JP 10248051 A WO 9839919 A1,

Relevance Rank: 93

Entry 13 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1998-496210

DERWENT-WEEK: 199847

TITLE:
Digital video data transmission method - separately encoding high resolution and low resolution video signals and then multiplexing encoded signals with identification information

INVENTOR:UENO, T

PATENT-ASSIGNEE: MATSUSHITA DENKI SANGYO KK[MATU], MATSUSHITA ELECTRIC IND CO LTD[MATU]

PRIORITY-DATA: 1997JP-0050154 (March 5, 1997)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 10248051 A	September 14, 1998	N/A	046	H04N 007/08
WO 9839919 A1	September 11, 1998	J	090	H04N 007/08

DESIGNATED-STATES: CA US AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP10248051A	N/A	1997JP-0050154	March 5, 1997
WO 9839919A1	N/A	1998WO-JP00906	March 5, 1998

IPC: H04N005/44; H04N007/08 ; H04N007/081 ; H04N007/24

ABSTRACTED-PUB-NO:WO 9839919A
BASIC-ABSTRACT:The digital data which is to be transmitted includes low resolution video signals (4) encoded by a low resolution compression encoder (13) and high resolution video signals (5) encoded by high resolution compression encoder (16). The two sets of encoded signals are multiplexed with a packet including identification information on a program. At the receiving side (22) the two sets of data are identified and reproduced by respective decoders (28, 30). ADVANTAGE - Increases freedom to mix video data of different resolutions, increasing flexibility of programming

CHOSEN-DRAWING:Dwg.1/34

TITLE-TERMS:
DIGITAL VIDEO DATA TRANSMISSION METHOD SEPARATE ENCODE HIGH RESOLUTION LOW RESOLUTION VIDEO SIGNAL MULTIPLEX ENCODE SIGNAL IDENTIFY INFORMATION

DERWENT-CLASS: W02 W04

EPI-CODES: W02-F07; W04-P01A;
Non-CPI Secondary Accession Numbers:N1998-387570

Full | Citation | Review | Classification | Date | Reference

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6. Document ID: US 5191416 A,

Relevance Rank: 91

Entry 6 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1993-093486

DERWENT-WEEK: 199311

TITLE:
Video signal processing system eliminating temporal aliasing - converts low-resolution video signal to format for transfer to high-resolution film and preserves realistic effect of motion from original video signal

INVENTOR:DICKSON, S P; VILLARREAL, W M

PATENT-ASSIGNEE: PACIFIC TITLE & ART STUDIO[PACIN], POST GROUP INC& ART STUDIO[POSTN]

PRIORITY-DATA: 1991US-0637486 (January 4, 1991)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 5191416 A	March 2, 1993	N/A	018	H04N 007/01

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
US 5191416A	N/A	1991US-0637486	January 4, 1991

IPC: H04N007/01; H04N007/18 ; H04N011/20

ABSTRACTED-PUB-NO:US 5191416A
BASIC-ABSTRACT:The image processing appts. converts an input video signal having a succession of interlaced fields, each representing an image at a different time, to an output video signal having a succession of non-interlaced frames. The appts. has a background generator responsive to the interlaced input video signal and providing a succession of non-interlaced background frames, each based on two or more successive associated fields on the input video signal. A motion detector senses areas of motion in the input fields corresp. to each background frame and generates data indicating the direction and magnitude of motion for each detected area. A superposition device incorporates the detected areas of motion into each background frame, to produce a succession of non-interlaced frames constituting an output video signal that preserves the effect of any motion represented in the input video signal. ADVANTAGE - Reduces signals frame rate to level compatible with that of film to be produced.

CHOSEN-DRAWING:Dwg.2/11B

TITLE-TERMS:
VIDEO SIGNAL PROCESS SYSTEM ELIMINATE TEMPORAL ALIASING CONVERT LOW RESOLUTION VIDEO SIGNAL FORMAT TRANSFER HIGH RESOLUTION FILM PRESERVE REALISTIC EFFECT MOTION ORIGINAL VIDEO SIGNAL

ADDL-INDEXING-TERMS:
CUBIC SPLINE ALGORITHM

DERWENT-CLASS: S06 W04

EPI-CODES: S06-B05; W04-D10; W04-H05; W04-N05A;
Non-CPI Secondary Accession Numbers:N1993-071585

7. Document ID: JP 06141296 A,

Relevance Rank: 91

Entry 7 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1994-204629

DERWENT-WEEK: 199425

TITLE:
Hierarchical pictorial-image coding method - has line interpolation between signal of each field which decomposes video signal into two or more signal components for improved clarity of low resolution video signals NoAbstract

PATENT-ASSIGNEE: MITSUBISHI ELECTRIC CORP[MITQ]

PRIORITY-DATA: 1992JP-0309660 (October 23, 1992)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 06141296 A	May 20, 1994	N/A	007	H04N 007/13

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP06141296A	N/A	1992JP-0309660	October 23, 1992

IPC: G06F015/66; H04N007/13 ; H04N011/04
ABSTRACTED-PUB-NO:JP06141296A
EQUIVALENT-ABSTRACT:

CHOSEN-DRAWING:Dwg.1/21

TITLE-TERMS:
HIERARCHY PICTURE IMAGE CODE METHOD LINE INTERPOLATION SIGNAL FIELD DECOMPOSE VIDEO SIGNAL TWO MORE SIGNAL COMPONENT IMPROVE CLEAR LOW RESOLUTION VIDEO SIGNAL NOABSTRACT

DERWENT-CLASS: T01 U21 W02 W04

EPI-CODES: T01-D02; T01-J10B; U21-A05A2; W02-F07; W04-P01A;
Non-CPI Secondary Accession Numbers:N1994-161293

Full | Citation | Review | Classification | Date | Reference

8. Document ID: EP 270235 A AU 8780516 A DK 8705653 A JP 63172581 A US 4875107 A US 5010419 A,

Relevance Rank: 89

Entry 1 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1988-156427

DERWENT-WEEK: 198823

TITLE:
Combined video camera and low resolution tape recording system - records low bandwidth FM signal on standard audio cassette tape and replays using rate conversion memory

INVENTOR:FANTONE, S D; HEIDT, T

PATENT-ASSIGNEE: WICKSTEAD J C[WICKI]

PRIORITY-DATA: 1986US-0938087 (December 4, 1986) , 1988US-0938087 (December 4, 1988) , 1989US-0378749 (July 23, 1989)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
EP 270235 A	June 8, 1988	E	018	N/A
AU 8780516 A	June 9, 1988	N/A	000	N/A
DK 8705653 A	June 5, 1988	N/A	000	N/A
JP 63172581 A	July 16, 1988	N/A	000	N/A
US 4875107 A	October 17, 1989	N/A	017	N/A
US 5010419 A	April 23, 1991	N/A	000	N/A

DESIGNATED-STATES: BE CH DE ES FR GB IT LI NL

CITED-DOCUMENTS: A3...9019; DE 2625154 ; DE 2900208 ; No-SR.Pub ; US 3922715 ; US 4131919 ; US 4133009 ; US 4263623 ; US 4475131 ; US 4544960 ; US 4546390

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
EP 270235A	N/A	1987EP-0309493	October 27, 1987
JP63172581A	N/A	1987JP-0282277	November 10, 1987
US 4875107A	N/A	1988US-0938087	December 4, 1988
US 5010419A	N/A	1989US-0378749	July 23, 1989

IPC: G11B020/00; H04N005/92 ; H04N007/12

ABSTRACTED-PUB-NO:EP 270235A
BASIC-ABSTRACT:The video appts. includes a camera (160) for converting light images into electrical video signals and a processor for converting the video signals into a low bandwidth frequency modulated storage signal with a bandwidth substantially lower than a standard TV video signal. A recording device (240) is provided to store the storage signal on an audio cassette, having a standard speed allowing storage of an audio bandwidth signal. The recording device has a drive for driving the cassette at higher than normal speed to increase the bandwidth storage capacity of the cassette, and a recording head for storing the storage signal on the cassette. ADVANTAGE - Highly portable and relatively low cost.

ABSTRACTED-PUB-NO:US 4875107A
EQUIVALENT-ABSTRACT:The video apparatus for storing video image on a recording medium and replaying the stored images on a display includes a camera which converts light images into electrical video signals. A processor coupled to the camera converts the electronic video signals into a low bandwidth frequency modulated storage signal with the bandwidth substantially lower than in a standard television video signal. A recorder coupled to the processor stores the low bandwidth frequency modulated storage signal on an audio cassette, which has a standard speed allowing storage of an audio bandwidth signal. The recorder includes a drive for driving the cassette at higher than normal speed to increase the bandwidth storage capacity of the cassette. The video apparatus also includes a switch mechanism for switching the video apparatus from a record mode where video images are stored on the cassette to a playback mode where the stored

images are read off the cassette and displayed on the video display. In the playback mode, the low bandwidth video signal is converted to a higher frequency standard television bandwidth video signal for display. USE/ADVANTAGE - Camcorder. Low resolution. (17pp) The video apparatus for storing video images on a recording medium has a camera converting light images into electrical video signals. A processor coupled to the camera includes appts. for converting the electronic video signal into a low bandwidth frequency modulated analog storage signal with a bandwidth lower than a standard television video signal. A recording medium coupled to the processor stores the low bandwidth frequency modulated analog storage signal on an audio cassette having a standard speed allowing storage of an audio band-width signal. The recording incudes a driver for driving the audio cassette at higher than normal speed to increase the bandwidth storage capacity of the audio cassette and recording head for storing the low bandwidth frequency modulated analog storage signal on the audio cassette. The camera includes a lens for focusing light and an integrator for integrating the light focused by the lens and the camera inputting the electrical video signals directly to the processors. USE/ADVANTAGE - CCD based portable camcorder. Low resolution video and audio recording and playback at low cost. (14pp)

CHOSEN-DRAWING:Dwg.2/10

TITLE-TERMS:
COMBINATION VIDEO CAMERA LOW RESOLUTION TAPE RECORD SYSTEM RECORD LOW BANDWIDTH FM SIGNAL STANDARD AUDIO CASSETTE TAPE REPLAY RATE CONVERT MEMORY

DERWENT-CLASS: W04

EPI-CODES: W04-B01; W04-B10; W04-F01; W04-M01X; W04-P01C;
Non-CPI Secondary Accession Numbers:N1988-119532

Full | Citation | Review | Classification | Date | Reference

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9. Document ID: EP 280932 A DE 3875983 G EP 280932 B1 JP 64000591 A US 4866520 A,

Relevance Rank: 89

Entry 2 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1988-251545

DERWENT-WEEK: 198836

TITLE:
Video signal display method for higher resolution monitor - cyclically selecting odd even and interpolated lines in preselected pattern to increase number of lines per picture

INVENTOR:MACHIDA, T; NOMURA, K ; TAKEKOSHI, T ; YAMADA, K

PATENT-ASSIGNEE: HITACHI LTD[HITA]

PRIORITY-DATA: 1987JP-0047536 (March 4, 1987)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
EP 280932 A	September 7, 1988	E	018	N/A
DE 3875983 G	December 24, 1992	N/A	000	H04N 007/01

EP 280932 B1	November 19, 1992	E	023	H04N 007/01
JP 64000591 A	January 5, 1989	N/A	000	N/A
US 4866520 A	September 12, 1989	N/A	016	N/A

DESIGNATED-STATES: DE FR GB DE FR GB

CITED-DOCUMENTS: EP 111362; GB 1525915 ; GB 1592486 ; GB 2090505 ; 01Jnl.Ref

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
EP 280932A	N/A	1988EP-0101882	February 9, 1988
DE 3875983G	N/A	1988DE-3875983	February 9, 1988
DE 3875983G	N/A	1988EP-0101882	February 9, 1988
DE 3875983G	Based on	EP 280932	N/A
EP 280932B1	N/A	1988EP-0101882	February 9, 1988
JP64000591A	N/A	1988JP-0047443	March 2, 1988
US 4866520A	N/A	1988US-0161782	February 29, 1988

IPC: G09G001/00; H04N003/22 ; H04N007/01

ABSTRACTED-PUB-NO:EP 280932A

BASIC-ABSTRACT:Each line of the lower resolution video signal is digitised to create a preselected number of digital values. Write address circuit determines appropriate memory addresses for each digital value. The addresses are indicative indicative of the line number within the picture or frame and of the position along the line. A memory (20a,20b) stores each digital value at the determined address. Read address circuit addresses are stored data in the memory at a rate controlled by the higher resolution video monitor to retrieve selected complete even and odd numbered lines of digital values. Odd line memory (20a) receives and temporarily holds each odd numbered raster line of digital values retrieved from the memory and even line memory (20b) and hold each even numbered line. An interpolating circuit (22) is connected with the even and odd line memories for interpolating the lines held. A circuit (24) cyclically selects among even, odd, and interpolated lines of data for display on the high resolution video monitor. USE/ADVANTAGE - Converts lower resolution video signals having raster lines of analog data into higher resolution video signal having larger number of raster lines. Particularly for displaying lower resolution interlaced TV signals on higher resolution CRT displays e.g. of computer monitors, without non-linear stretching of image and without line repetitions.

ABSTRACTED-PUB-NO:EP 280932B

EQUIVALENT-ABSTRACT:A method for converting an interlaced field lower resolution video signal having sequentially an odd numbers field comprising the odd-numbere d raster lines of a scanned picture in the form of analog data and an even numbers field comprising the even-numbered raster lines of a scanned picture in the form of analog data into a higher resolution video signal having sequential fields, each having a larger plurality of raster lines, the lower resolution video signal representing a picture consisting of a plurality of consecutive raster lines which are numbered consecutively, the method comprising the following steps: digitising each analog raster line of odd numbers and even numbers fields of the lower resolution video signal into a pre-selected plurality of digital values; characterised in further comprising the steps of: storing the digital values in accordance with the low resolution video signal field, line number and position within the line selectively reading digital values corresponding to adjacent raster lines in the picture; interpolating the read digital values to obtain digital values for raster lines of the higher resolution video signal; and assembling the interpolated lines and at least one of the odd numbers and even numbers field raster lines for each field of the highe The appts. comprises a A/D converter (44) assigning received lines of each even and odd line fields to given digital values. A write address circuit (56) determines a memory address m corresponding to each digital value, indicating the field, then (46) stores the digital values in conjunction

with the corresp. address. The memory is converted to the A/D converter and write address circuits. A read address circuit (72) addresses the memory to read digital values of the selected lines of the odd and even line fields. An odd line field memory (20A) and even line field memory (20B) receive and hold lines of their respective fields digital values from the buffer. An interpolator (22) takes the even and odd line digital values and produce an interpolated line. A selected (24) cyclically takes a mix of even field, odd field and interpolated lines for display in a common higher resolution field on the video monitor. USE/ADVANTAGE - Computer CRT displays, video displays. Magnifies displayed picture of video signal. Improves apparant resolution of signal. Reduced distortion, improved definition, higher quality of picture. (16pp)

CHOSEN-DRAWING:Dwg.1/12

TITLE-TERMS:
VIDEO SIGNAL DISPLAY METHOD HIGH RESOLUTION MONITOR CYCLIC SELECT ODD EVEN INTERPOLATION LINE PRESELECTED PATTERN INCREASE NUMBER LINE PER PICTURE

DERWENT-CLASS: P85 T04 W03

EPI-CODES: T04-H01; W03-A11; W03-A20;
Non-CPI Secondary Accession Numbers:N1988-191335

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10. Document ID: DE 3629462 A DE 3629462 C2 GB 2195858 A JP 63061575 A US 4825296 A CH 674269 A GB 2195858 B JP 07154727 A,

Relevance Rank: 89

Entry 3 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1988-065071

DERWENT-WEEK: 199624

TITLE:
Electronic image processing system for CRT printer - has image store in front and behind image processor with parallel store supplying display monitor

INVENTOR:FUCHSBERGE, H; RUF, W ; WAGENSONNE, E ; FUCHSBERGER, H ; WAGENSONNER, E

PATENT-ASSIGNEE: AGFA-GEVAERT AG[GEVA]

PRIORITY-DATA: 1986DE-3629462 (August 29, 1986)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
DE 3629462 A	March 3, 1988	N/A	004	N/A
DE 3629462 C2	May 15, 1996	N/A	006	H04N 001/00
GB 2195858 A	April 13, 1988	N/A	000	N/A
JP 63061575 A	March 17, 1988	N/A	000	N/A
US 4825296 A	April 25, 1989	N/A	007	N/A
CH 674269 A	May 15, 1990	N/A	000	N/A
GB 2195858 B	May 15, 1991	N/A	000	N/A
JP 07154727 A	June 16, 1995	N/A	006	H04N 005/76

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
DE 3629462A	N/A	1986DE-3629462	August 29, 1986
DE 3629462C2	N/A	1986DE-3629462	August 29, 1986
GB 2195858A	N/A	1987GB-0020315	August 28, 1987
JP63061575A	N/A	1987JP-0204312	August 19, 1987
US 4825296A	N/A	1987US-0085941	August 14, 1987
JP07154727A	Div ex	1987JP-0204312	August 19, 1987
JP07154727A	N/A	1994JP-0187025	August 19, 1987

IPC: G01T005/00; G03B027/80 ; G06F015/62 ; H04N001/00 ; H04N001/21 ; H04N005/76 ; H04N005/91

ABSTRACTED-PUB-NO:DE 3629462A
BASIC-ABSTRACT:The processing system receives the image signals obtained by electro-optic al scanning of a 2-dimensional original and supplies the corrected image signals to a CRT printer (3) for providing a positive copy. The image signal sequence is entered in a respective image store (6,7) before and after the image processor (4), with a further image store (9) for the corrected image signals coupled to a display monitor (11) for visual examination of the image. Pref. a further image processor (10) is inserted between the auxiliary image store (9) and the display monitor (11). ADVANTAGE - Increased image processing speed.

ABSTRACTED-PUB-NO:GB 2195858B
EQUIVALENT-ABSTRACT:A method of electronic image processing comprising the steps of electro-optically scanning a two-dimensional original point by point; generating raw imaging signals based on the scanning step, each pixel being accorded a respective density value; transmitting said raw signals along a predetermined path; storing said raw signals in a first part of said path; correcting the raw image signals in an image processor in a second part of said path downstream of said first part; storing the corrected signals in a third part of said path downstream of said second part; converting the corrected signals into a printable image in a fourth parth of said path downstream of said third part; and wherein each of said first part of said path is performed for an additional original, the raw signals for said additional original being stored prior to the correcting steps for said additional original at a location other than said first part of said path. An original to be copied is electrooptically scanned point-by-point. The resulting imaging signals are stored in a memory and then forwarded to an image processing unit where the signals are electronically corrected to enhance the image of the original. The corrected signals are loaded into a second memory. A portion of the corrected signals is recalled from the second memory and sent to a third memory. The portion of the corrected signals is then transmitted to a second image processing unit and converted into a low-resolution video-image which can be inspected to determine image quality. If image quality is satisfactory, the contents of the second memory are sent to an exposure unit which prints a high-resolution image of the original on copy material. Imaginq signals for a second original are loaded into the first memory as the contents of the second memory are recalled for printinq. The second processing unit functions to adjust the vide image so that it closely corresponds to the printed image of the original. (7pp)

CHOSEN-DRAWING:Dwg.1/1

TITLE-TERMS:
ELECTRONIC IMAGE PROCESS SYSTEM CRT PRINT IMAGE STORAGE FRONT IMAGE PROCESSOR PARALLEL STORAGE SUPPLY DISPLAY MONITOR

DERWENT-CLASS: P82 S06 W02 W04

EPI-CODES: S06-C02; W02-J03A; W02-J04; W04-D10;
Non-CPI Secondary Accession Numbers:N1988-049277

Full | Citation | Review | Classification | Date | Reference

11. Document ID: EP 627859 A2 EP 627859 A3 JP 07099646 A,

Relevance Rank: 89

Entry 8 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1995-008355

DERWENT-WEEK: 199502

TITLE:
Encoding and/or decoding appts for digital video signals - produces two hierarchical data signals representing e.g. conventional TV and HDTV signals

INVENTOR:FUJIMORI, Y; KAWAGUCHI, K ; KONDO, T

PATENT-ASSIGNEE: SONY CORP[SONY]

PRIORITY-DATA: 1993JP-0237431 (August 30, 1993) , 1993JP-0152836 (May 31, 1993)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
EP 627859 A2	December 7, 1994	E	018	H04N 007/13
EP 627859 A3	March 8, 1995	N/A	000	H04N 007/13
JP 07099646 A	April 11, 1995	N/A	009	H04N 007/24

DESIGNATED-STATES: DE FR GB

CITED-DOCUMENTS: No-SR.Pub; 2.Jnl.Ref ; EP 392753 ; EP 497058 ; US 4222076 ; US 5136391

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
EP 627859A2	N/A	1994EP-0303869	May 27, 1994
EP 627859A3	N/A	1994EP-0303869	May 27, 1994
JP07099646A	N/A	1993JP-0237431	August 30, 1993

IPC: G06T009/00; H04N007/13 ; H04N007/24

ABSTRACTED-PUB-NO:EP 627859A

BASIC-ABSTRACT:The apparatus produces at least two hierarchical data signals which respectively represent two (low resolution) video signals. A circuit (2) receives the input digital video signal and generates the second hierarchical data signal by calculating each pixel data signal of the second hierarchical data signal as a linear combination of N pixel data signals of the input digital video signal. A circuit (7,8) outputs the generated second hierarchical data signal together with the first hierarchical pixel data signals representing only N-1 of the N pixel data signals of the input digital video signal. Also claims a decoding apparatus. ADVANTAGE - Allows hierarchical encoding and/or decoding on digital image signal without reducing encoding efficiency and with decreased delay and hardware scale on decoding side.

CHOSEN-DRAWING:Dwg.1/9

TITLE-TERMS:
ENCODE DECODE APPARATUS DIGITAL VIDEO SIGNAL PRODUCE TWO HIERARCHY DATA SIGNAL REPRESENT CONVENTION TELEVISION HDTV SIGNAL

DERWENT-CLASS: W02 W04

EPI-CODES: W02-F06C; W04-P01A;
Non-CPI Secondary Accession Numbers:N1995-006955

Full | Citation | Review | Classification | Date | Reference

12. Document ID: US 5592299 A,

Relevance Rank: 89

Entry 11 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1997-086846

DERWENT-WEEK: 199708

TITLE:
Video image representation data reduction method - representing pair of field pictures by single field and preventing second field display by setting digital storage media byte

INVENTOR:BOYCE, J M; LANE, F A ; PEARLSTEIN, L

PATENT-ASSIGNEE: HITACHI AMERICA LTD[HITA]

PRIORITY-DATA: 1994US-0311811 (September 26, 1994)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 5592299 A	January 7, 1997	N/A	014	H04N 005/76

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
US 5592299A	N/A	1994US-0311811	September 26, 1994

IPC: H04N005/76; H04N005/78 ; H04N009/79

RELATED-ACC-NO: 1997-549150

ABSTRACTED-PUB-NO:US 5592299A
BASIC-ABSTRACT: A compressed HDTV digital video data stream is received, which includes a pair of field pictures. Both are represented by digital data. One of the field pictures of the pair is replaced by a third picture, represented by less digital data than the picture being replaced. The third picture is a transparent field. Header information associated with the pair of field pictures is generated, this being a digital storage media control byte. The byte includes a control bit set to prevent a receiver from displaying the third picture. The first and third pictures are recorded on a tape, in a tape segment from which the data can be read during the fast forward operation of a digital tape recorder. USE/ADVANTAGE - For processing digital video data to reduce amount of data required to represent a video frame. Low resolution video frames suitable for recording in trick play tape segments. No additional data needed to support trick play mode. Minimal flicker in trick play mode.

CHOSEN-DRAWING:Dwg.2/3

TITLE-TERMS:
VIDEO IMAGE REPRESENT DATA REDUCE METHOD REPRESENT PAIR FIELD PICTURE SINGLE FIELD PREVENT SECOND FIELD DISPLAY SET DIGITAL STORAGE MEDIUM BYTE

DERWENT-CLASS: W04

EPI-CODES: W04-F01;
Non-CPI Secondary Accession Numbers:N1997-071601

Full | Citation | Review | Classification | Date | Reference

13. Document ID: US 5793414 A,

Relevance Rank: 89

Entry 12 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1998-456397

DERWENT-WEEK: 199839

TITLE:
Interactive video communication system - includes printer processor which converts viewer selected relatively high resolution colour digital image to control signal for printing image on system user's dumb colour printer

INVENTOR:SHAFFER, S L

PATENT-ASSIGNEE: EASTMAN KODAK CO[EAST]

PRIORITY-DATA: 1995US-0559388 (November 15, 1995)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 5793414 A	August 11, 1998	N/A	007	H04N 007/16

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
US 5793414A	N/A	1995US-0559388	November 15, 1995

IPC: H04N007/14; H04N007/16

ABSTRACTED-PUB-NO:US 5793414A
BASIC-ABSTRACT:The system includes a central information facility connected to a communication channel. An interactive information database contains relatively low resolution video programming material with imbedded references to relatively high resolution colour digital images selectable by a system user. A printer processor (24) converts a viewer selected relatively high resolution colour digital image to control signals for printing the image on a system user's dumb colour printer. Multiple system users are also included, each of which is provided with a transceiver, a video display, a dumb colour printer (26) and a controller (16). The high resolution digital images referenced in the programming materials are selected by the controller. ADVANTAGE - Avoids need for dumb printer to incorporate data buffer or raster image buffer or raster image processor thereby saving expenses of such electronic units in printer. Changes system user's printer without need to reprocess images in interactive database.

CHOSEN-DRAWING:Dwg.1/3

TITLE-TERMS:
INTERACT VIDEO COMMUNICATE SYSTEM PRINT PROCESSOR CONVERT VIEW SELECT RELATIVELY HIGH RESOLUTION COLOUR DIGITAL IMAGE CONTROL SIGNAL PRINT IMAGE SYSTEM USER DUMB COLOUR PRINT

DERWENT-CLASS: W02 W04

EPI-CODES: W02-F10A; W02-F10X; W04-D10;
Non-CPI Secondary Accession Numbers:N1998-356150

14. Document ID: JP 10222133 A,

Relevance Rank: 89

Entry 14 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1998-511109

DERWENT-WEEK: 199844

TITLE:
Drive circuit for liquid crystal display device - includes D-flip flop to divide sampling clock of frequency of 25MHz to 12.5MHz, exclusive OR gate to generate new clock signal by EX-OR divided signal with clock from timing generator

PATENT-ASSIGNEE: SONY CORP[SONY]

PRIORITY-DATA: 1997JP-0027060 (February 10, 1997)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 10222133 A	August 21, 1998	N/A	009	G09G 003/36

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP10222133A	N/A	1997JP-0027060	February 10, 1997

IPC: G09G003/36; G09G005/00 ; G09G005/18 ; H04N005/66

ABSTRACTED-PUB-NO:JP10222133A
BASIC-ABSTRACT:The drive circuit includes a D-flip flop (11) which divides the sampling clock of frequency of 25MHz to a signal of frequency of 12.5MHz. The divided signal is input to an EX-OR gate (12), which EX-OR's this signal with clock from timing generator and generates a new clock signal. A video signal output unit then outputs video signal to the liquid crystal display device, synchronised with the new clock signal. ADVANTAGE - Reduces power consumption. Suppresses degradation of image quality, when low resolution video is displayed by high resolution liquid crystal display device.

CHOSEN-DRAWING:Dwg.2/11

TITLE-TERMS:
DRIVE CIRCUIT LIQUID CRYSTAL DISPLAY DEVICE FLIP DIVIDE SAMPLE CLOCK FREQUENCY EXCLUDE GATE GENERATE NEW CLOCK SIGNAL DIVIDE SIGNAL CLOCK TIME GENERATOR

DERWENT-CLASS: P85 T04 W03

EPI-CODES: T04-H03B; T04-H03C2A; W03-A08;
Non-CPI Secondary Accession Numbers:N1998-398822

Full | Citation | Review | Classification | Date | Reference

Term	Documents
low adj resolution adj video	14

Display Documents Starting At: 1

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#	Patent	Source	Flag	Issue Date	Pages	Current Original Classif	Retrieval Classif	Current Cross Reference
1	5,844,538	U	U	12/01/1998	34	345/98		345/87 ...
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3	5,828,367	U	U	10/27/1998	10	345/211		345/87 ...
4	5,825,341	U	U	10/20/1998	9	345/87		345/59 ...
5	5,818,411	U	U	10/06/1998	21	345/99		345/87 ...
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7	5,815,131	U	U	09/29/1998	14	345/94		345/99 ...
8	5,790,090	U	U	08/04/1998	9	345/94		345/98 ...
9	5,786,800	U	U	07/28/1998	39	345/98		345/99
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13	5,757,346	U	U	05/26/1998	11	345/87		345/98
14	5,757,342	U	U	05/26/1998	13	345/60		345/87 ...
15	5,754,151	U	U	05/19/1998	6	345/92		345/87 ...
16	5,751,267	U	U	05/12/1998	20	345/96		345/87 ...
17	5,748,167	U	U	05/05/1998	48	345/98		345/99
18	5,748,162	U	U	05/05/1998	12	345/87		345/94 ...
19	5,742,269	U	U	04/21/1998	9	345/87		345/94 ...
20	5,736,981	U	U	04/07/1998	58	345/507		345/87 ...
21	5,731,796	U	U	03/24/1998	75	345/96		345/87 ...
22	5,726,673	U	U	03/10/1998	10	345/87		345/94 ...
23	5,719,590	U	U	02/17/1998	19	345/94		345/99
24	5,708,454	U	U	01/13/1998	23	345/100		345/87 ...
25	5,708,453	U	U	01/13/1998	18	345/87		341/126 ...
26	5,699,076	U	U	12/16/1997	26	345/103		345/93 ...
27	5,682,176	U	U	10/28/1997	10	345/98		345/99
28	5,682,175	U	U	10/28/1997	13	345/98		345/99 ...
29	5,680,149	U	U	10/21/1997	13	345/98		345/87
30	5,675,351	U	U	10/07/1997	18	345/87		345/94 ...
31	5,668,567	U	U	09/16/1997	10	345/60		345/87 ...
32	5,657,041	U	U	08/12/1997	26	345/99		345/94
33	5,657,037	U	U	08/12/1997	20	345/94		345/78 ...
34	5,644,331	U	U	07/01/1997	11	345/99		345/98 ...
35	5,629,718	U	U	05/13/1997	8	345/99		345/94 ...
36	5,627,559	U	U	05/06/1997	9	345/97		345/87 ...
37	5,623,279	U	U	04/22/1997	25	345/98		307/404 ...
38	5,619,225	U	U	04/08/1997	34	345/98		345/88 ...
39	5,614,923	U	U	03/25/1997	10	345/99		345/95 ...
40	5,610,627	U	U	03/11/1997	34	345/99		345/87 ...
41	5,608,420	U	U	03/04/1997	18	345/89		345/94 ...
42	5,602,560	U	U	02/11/1997	13	345/94		345/58 ...
43	5,598,179	U	U	01/28/1997	21	345/98		345/94 ...
44	5,589,847	U	U	12/31/1996	23	345/98		345/87
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46	5,552,801	U	U	09/03/1996	18	345/100		345/87 ...
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51	5,519,414	U	U	05/21/1996	24	345/208		345/94	...
52	5,515,080	U	U	05/07/1996	14	345/509		345/87	...
53	5,489,917	U	U	02/06/1996	14	345/89		345/87	...
54	5,483,255	U	U	01/09/1996	68	345/98		345/87	
55	5,481,273	U	U	01/02/1996	11	345/94		345/87	...
56	5,459,482	U	U	10/17/1995	22	345/98		345/87	...
57	5,448,259	U	U	09/05/1995	12	345/99		345/98	
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61	5,283,564	U	U	02/01/1994	12	345/87		345/94	...
62	5,253,091	U	U	10/12/1993	10	345/94		345/87	...
63	5,244,596	U	U	09/14/1993	156	345/87		252/299.01	...
64	5,243,454	U	U	09/07/1993	6	345/87		345/94	
65	5,181,131	U	U	01/19/1993	6	345/87		345/97	...
66	5,170,156	U	U	12/08/1992	32	345/85		345/87	...
67	5,105,288	U	U	04/14/1992	9	345/87		345/94	
68	5,093,736	U	U	03/03/1992	14	345/87		345/94	
69	4,902,105	U	U	02/20/1990	8	345/94		345/87	
70	4,754,271	U	U	06/28/1988	8	345/98		345/87	...
71	4,748,444	U	U	05/31/1988	17	345/99		345/94	...
72	4,743,896	U	U	05/10/1988	6	345/87		345/98	
73	4,617,563	U	U	10/14/1986	7	345/87		345/98	
74	4,574,282	U	U	03/04/1986	12	345/87		345/94	...
75	4,506,955	U	U	03/26/1985	9	345/87		345/94	...
76	4,449,125	U	U	05/15/1984	7	345/87		345/98	...
77	4,352,102	U	U	09/28/1982	3	345/94		345/99	...
78	4,275,421	U	U	06/23/1981	17	348/589		345/98	...
79	4,040,719	U	U	08/09/1977	8	345/87		334/86	...
80	4,028,692	U	U	06/07/1977	9	345/87		340/825.81	...
81	3,861,782	U	U	01/21/1975	8	345/87		252/299.5	...
82	3,776,615	U	U	12/04/1973	11	345/87		340/825.81	...

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50	5,375,203	U	U	12/20/1994	11	345/511		345/515	...
51	5,369,734	U	U	11/29/1994	19	345/421		345/419	...
52	5,369,262	U	U	11/29/1994	16	345/179		235/440	...
53	5,361,081	U	U	11/01/1994	19	345/145		345/157	
54	5,355,496	U	U	10/11/1994	88	395/706		364/280	...
55	5,335,321	U	U	08/02/1994	11	345/503		345/204	
56	5,326,878	U	U	07/05/1994	6	548/315.1		548/317.1	...
57	5,317,331	U	U	05/31/1994	11	345/16		345/13	
58	5,306,726	U	U	04/26/1994	20	514/375		548/217	
59	5,300,944	U	U	04/05/1994	30	345/88		345/152	
60	5,300,926	U	U	04/05/1994	12	345/157		345/145	...
61	5,293,482	U	U	03/08/1994	12	345/517			
62	5,274,758	U	U	12/28/1993	25	345/302			
63	5,232,945	U	U	08/03/1993	18	514/456		514/374	...
64	5,227,863	U	U	07/13/1993	83	348/578		345/302	...
65	5,191,416	U	U	03/02/1993	18	348/459	PARTIAL DISPlay		
66	5,179,320	U	U	01/12/1993	12	315/399			
67	5,168,456	U	U	12/01/1992	29	364/728.03		364/726.02	
68	5,119,474	U	U	06/02/1992	25	345/302			
69	5,089,514	U	U	02/18/1992	14	514/374		514/253	...
70	5,084,392	U	U	01/28/1992	6	435/280		435/125	...
71	5,065,346	U	U	11/12/1991	7	345/428		345/115	...
72	5,051,981	U	U	09/24/1991	12	370/290		341/144	...
73	5,051,929	U	U	09/24/1991	16	345/431		345/150	...
74	5,048,077	U	U	09/10/1991	12	379/93.17		348/14	...
75	5,043,810	U	U	08/27/1991	32	348/413		348/399	
76	5,023,905	U	U	06/11/1991	13	379/93.17		340/825.4	...
77	4,972,396	U	U	11/20/1990	8	369/32		360/18	...
78	4,960,910	U	U	10/02/1990	7	549/510		544/264	...
79	4,952,951	U	U	08/28/1990	14	347/130		347/118	...
80	4,922,240	U	U	05/01/1990	23	345/100		345/205	
81	4,912,042	U	U	03/27/1990	6	435/145		435/135	...
82	4,888,795	U	U	12/19/1989	48	348/18		348/19	...
83	4,875,036	U	U	10/17/1989	7	345/104		178/18.01	...
84	4,866,520	U	U	09/12/1989	16	348/441		345/136	
85	4,839,634	U	U	06/13/1989	57	345/173		178/18.09	...
86	4,827,085	U	U	05/02/1989	31	345/174		345/104	...
87	4,825,301	U	U	04/25/1989	10	386/121		348/311	...
88	4,790,629	U	U	12/13/1988	15	345/150		84/464R	...
89	4,785,296	U	U	11/15/1988	22	345/129		345/132	...
90	4,780,760	U	U	10/25/1988	8	348/397		348/412	...
91	4,769,636	U	U	09/06/1988	26	345/340		345/342	...
92	4,751,507	U	U	06/14/1988	10	345/340		345/131	...
93	4,745,474	U	U	05/17/1988	8	348/419		375/244	
94	4,744,042	U	U	05/10/1988	27	364/726.02		968/900	...
95	4,739,414	U	U	04/19/1988	42	358/482		358/496	...
96	4,728,803	U	U	03/01/1988	47	358/465	DISPlay	358/482	...

#	Patent	Source	Flag	Issue Date	Pages	Current Original Classif	Retrieval Classif	Current Cross Reference
1	5,844,539	U	U	12/01/1998	12	345/100		345/132 ...
2	5,841,438	U	U	11/24/1998	16	345/348		345/302 ...
3	5,841,435	U	U	11/24/1998	24	345/339		345/329 ...
4	5,832,112	U	U	11/03/1998	121	382/181		382/299
5	5,819,010	U	U	10/06/1998	57	395/109		358/447 ...
6	5,812,135	U	U	09/22/1998	10	345/356		707/100
7	5,808,624	U	U	09/15/1998	66	345/435		
8	5,805,461	U	U	09/08/1998	84	364/488		364/578 ...
9	5,798,796	U	U	08/25/1998	12	348/405		348/438
10	5,798,748	U	U	08/25/1998	24	345/156		345/165 ...
11	5,754,169	U	U	05/19/1998	15	345/173		345/157 ...
12	5,751,338	U	U	05/12/1998	51	348/17		345/2 ...
13	5,729,358	U	U	03/17/1998	61	358/451		395/102
14	5,717,414	U	U	02/10/1998	12	345/8		345/7 ...
15	5,714,985	U	U	02/03/1998	22	345/508		
16	5,710,721	U	U	01/20/1998	13	395/185.04		395/183.19 ...
17	5,710,576	U	U	01/20/1998	11	345/169		345/901 ...
18	5,706,027	U	U	01/06/1998	25	345/156		73/862.043 ...
19	5,703,604	U	U	12/30/1997	23	345/8		348/36 ...
20	5,686,934	U	U	11/11/1997	18	345/97		345/99
21	5,677,708	U	U	10/14/1997	19	345/115		345/123 ...
22	5,640,543	U	U	06/17/1997	15	345/502		345/508 ...
23	5,640,131	U	U	06/17/1997	48	332/109		327/176 ...
24	5,629,696	U	U	05/13/1997	46	341/101		
25	5,629,332	U	U	05/13/1997	15	514/383		514/340 ...
26	5,611,038	U	U	03/11/1997	86	345/302		345/327 ...
27	5,604,861	U	U	02/18/1997	19	345/326		345/348 ...
28	5,597,808	U	U	01/28/1997	19	514/33		536/18.1
29	5,589,993	U	U	12/31/1996	16	386/81		348/390 ...
30	5,579,458	U	U	11/26/1996	10	345/433		345/507
31	5,579,412	U	U	11/26/1996	16	382/240		382/299
32	5,572,732	U	U	11/05/1996	84	395/701		364/280 ...
33	5,563,996	U	U	10/08/1996	35	707/521		345/341 ...
34	5,555,002	U	U	09/10/1996	13	345/121		345/127
35	5,530,457	U	U	06/25/1996	15	345/507		345/1 ...
36	5,502,419	U	U	03/26/1996	51	332/109		327/74 ...
37	5,491,789	U	U	02/13/1996	12	395/183.01		364/267 ...
38	5,488,698	U	U	01/30/1996	16	395/110		345/441 ...
39	5,477,397	U	U	12/19/1995	17	386/123		348/390 ...
40	5,459,514	U	U	10/17/1995	14	348/398		348/387 ...
41	5,438,074	U	U	08/01/1995	19	514/456		549/398
42	5,432,525	U	U	07/11/1995	33	345/2		
43	5,430,838	U	U	07/04/1995	11	345/344		345/340 ...
44	5,425,050	U	U	06/13/1995	26	375/200		380/10 ...
45	5,422,987	U	U	06/06/1995	20	345/427		345/163 ...
46	5,406,302	U	U	04/11/1995	9	345/55		340/815.41 ...
47	5,398,310	U	U	03/14/1995	24	707/541		345/341 ...
48	5,398,143	U	U	03/14/1995	8	360/48		

#	Patent	Source	[redacted]	Issue Date	Pages	Current Original Classif	[redacted]etrieval Classif	Current Cross Reference
1	5,819,010	U	T	10/06/1998	57	395/109		358/447 ...
2	5,798,748	U	T	08/25/1998	24	345/156		345/165 ...
(3)	5,736,981	U	T	04/07/1998	58	345/507		345/87 ...
4	5,729,358	U	T	03/17/1998	61	358/451		395/102
5	5,714,985	U	T	02/03/1998	22	345/508		
6	5,710,721	U	T	01/20/1998	13	395/185.04		395/183.19 ...
7	5,579,412	U	T	11/26/1996	16	382/240		382/299
8	5,477,397	U	T	12/19/1995	17	386/123		348/390 ...
9	5,444,834	U	T	08/22/1995	19	345/434		345/433
10	5,425,050	U	T	06/13/1995	26	375/200		380/10 ...
11	5,300,944	U	T	04/05/1994	30	345/88		345/152
12	5,293,482	U	T	03/08/1994	12	345/517		
13	5,227,863	U	T	07/13/1993	83	348/578		345/302 ...
14	5,191,416	U	T	03/02/1993	18	348/459		
15	5,065,346	U	T	11/12/1991	7	345/428		345/115 ...
16	5,051,929	U	T	09/24/1991	16	345/431		345/150 ...
17	4,888,795	U	T	12/19/1989	48	348/18		348/19 ...
18	4,866,520	U	T	09/12/1989	16	348/441		345/136
19	4,780,760	U	T	10/25/1988	8	348/397		348/412 ...
20	4,745,474	U	T	05/17/1988	8	348/419		375/244
21	4,656,468	U	T	04/07/1987	11	345/509		345/136
22	4,641,185	U	T	02/03/1987	8	358/535		358/513

Serial to Parallel Converter

```
=> s low resolution to high resolution

       1109689 LOW
        113650 RESOLUTION
       1416232 HIGH
        113650 RESOLUTION
L1         102 LOW RESOLUTION TO HIGH RESOLUTION
                 (LOW(W)RESOLUTION(1W)HIGH(W)RESOLUTION)

=> s serial to parallel

         88961 SERIAL
        856588 PARALLEL
L2       10329 SERIAL TO PARALLEL
                 (SERIAL(1W)PARALLEL)

=> s l1 and l2

L3           8 L1 AND L2

=> d kwic

US PAT NO:      5,481,275 [IMAGE AVAILABLE]              L3: 1 of 8

DETDESC:

DETD(11)

 The . . . "HR" and "HC" are used throughout to respectively represent
High-resolution Row and High-resolution Column. FIG. 2 shows the relation
between low-resolution and high-resolution rows and
columns.

DETDESC:

DETD(36)

 The . . . in FIG. 2 to show groups of four HPx's each associated with
a corresponding four subposition regions, QA-QD, of each
low-resolution pixel. High-resolution pixels 204 are
depicted as dashed (hidden) circles in FIG. 2.

DETDESC:

DETD(128)

 The . . . is that signals are repeatedly converted between parallel
and serial formats as they flow downstream through a pipelined
architecture. The parallel-to-serial-to-parallel conversions help
to reduce the die-size and pin count of the CLIO chip 430 and help to
take full advantage. . .

=> s 2 kwic

       2382668 2
            12 KWIC
<------User Break------>
```

u
SEARCH ENDED BY [redacted]

=>

=> d 2 kwic

US PAT NO: 5,090,026 [IMAGE AVAILABLE] L3: 2 of 8

DETDESC:

DETD(9)

The address generator 15 is illustrated in FIG. 2 as including a **serial**-to-**parallel** converter 18 using a **serial** in/**parallel** out eight-bit converter for the five most significant bits, and a interpolation counter 19 realizable as a five-stage binary counter. . . Clock at 90.degree. reclocks Tx Data by means of the D-type flip-flop 11, clocks differential encoder 3 and clocks the **serial**-to-**parallel** interface 18. In order to generate the Tx Clock at 0.degree. the Tx Clock at 90.degree. is converted using a. . .

DETDESC:

DETD(25)

Flip-flops . . . At high resolution, the HF Reference clock signal is not divided and provided directly to line 64. The selection of **low resolution** or **high resolution** is controlled by the Select Resolution signal on line 76. With a higher frequency loop clock signal on line 64,. . .

=> d 3 kwic

US PAT NO: 5,065,346 [IMAGE AVAILABLE] L3: 3 of 8

ABSTRACT:
A **low resolution** to **high resolution** display system arranged such that a low resolution video signal from a personal computer is written in a memory plane. . .

DETDESC:

DETD(5)

The display signal derived from the V-RAM 3 is supplied to the display circuit 200, and more specifically to a **serial**-to-**parallel** converting circuit 4 and a bit clock from the display controller 1 is also supplied to the **serial**-to-**parallel** converting circuit 4, whereby parallel data is formed by the **serial**-to-**parallel** converting circuit 4 at, for example, every 16 bits. This parallel data is supplied to a memory plane 5.

=> d 4 kwic

US PAT NO: 4,949,391 [IMAGE AVAILABLE] L3: 4 of 8

DETDESC:

DETD(149)

The . . . shown in the block diagram of FIG. 9D consists of the

control logic 435, the data reduction logic 440, the **serial**-in-**parallel**-out (SIPO) register 405 and the acquisition control state machine 450. The acquisition control state machine 450 runs asynchronously to any. . .

DETDESC:

DETD(156)

The . . . row address counter 330 (FIG. 9B) to provide the row and column addresses and support two addressing schemes which provide **low resolution** and **high resolution** image data.

DETDESC:

DETD(160)

The acquisition resolution mode (**low resolution**, uncompressed **high resolution** and compressed high resolution) is controlled by the central controller 50 (FIG. 1) by writing to the camera control register. . .

DETDESC:

DETD(161)

The . . . camera resolution mode selected, the wait time and the soak time. Table II shows maximum and minimum cycle times for **low resolution** and **high resolution** modes.

DETDESC:

DETD(162)

TABLE II

ACQUISITION CYCLE TIMES			
Low Resolution		**High Resolution**	
Min	Max	Min	Max
3.38 msec	9.86 msec	6.55 msec	13.03 msec

=> d 5 kwic

US PAT NO: 4,882,629 [IMAGE AVAILABLE] L3: 5 of 8

DETDESC:

DETD(148)

The . . . shown in the block diagram of FIG. 9D consists of the control logic 435, the data reduction logic 440, the **serial**-in-**parallel**-out (SIPO) register 405 and the acquisition control state machine 450. The acquisition control state machine 450 runs asynchronously to any. . .

DETDESC:

DETD(155)

The . . . row address counter 330 (FIG. 9B) to provide the row and

column addresses support two addressing schemes which provide **low resolution** and **high resolution** image data.

DETDESC:

DETD(159)

The acquisition resolution mode (**low resolution**, uncompressed **high resolution** and compressed high resolution) is controlled by the central controller 50 (FIG. 1) by writing to the camera control register. . .

DETDESC:

DETD(160)

The . . . camera resolution mode selected, the wait time and the soak time. Table II shows maximum and minimum cycle times for **low resolution** and **high resolution** modes.

DETDESC:

DETD(161)

TABLE II

ACQUISITION CYCLE TIMES			
Low Resolution		**High Resolution**	
Min	Max	Min	Max
3.38 msec	9.86 msec	6.55 msec	13.03 msec

=> d 1-8

1. 5,481,275, Jan. 2, 1996, Resolution enhancement for video display using multi-line interpolation; Robert J. Mical, et al., 345/132, 138, 149 [IMAGE AVAILABLE]

2. 5,090,026, Feb. 18, 1992, GMSK narrowband modem; Harold P. Stern, et al., 375/274; 329/300; 332/100; 375/296, 305, 336 [IMAGE AVAILABLE]

3. 5,065,346, Nov. 12, 1991, Method and apparatus for employing a buffer memory to allow low resolution video data to be simultaneously displayed in window fashion with high resolution video data; Toshihiko Kawai, et al., 345/428, 115, 132; 348/552 [IMAGE AVAILABLE]

4. 4,949,391, Aug. 14, 1990, Adaptive image acquisition system; James L. Faulkerson, et al., 382/313, 221 [IMAGE AVAILABLE]

5. 4,882,629, Nov. 21, 1989, Adaptive exposure control system; James L. Faulkerson, et al., 358/464, 447, 471; 382/321 [IMAGE AVAILABLE]

6. 4,851,834, Jul. 25, 1989, Multiport memory and source arrangement for pixel information; Thomas C. Stockebrand, et al., 345/509, 191, 198 [IMAGE AVAILABLE]

7. 4,734,769, Mar. 29, 1988, Method and apparatus for display of variable intensity pictures on a video display terminal; Mark A. Davis, 348/564, 461, 473, 589 [IMAGE AVAILABLE]

8. 4,654,484, Mar. 31, 1987, Video compression/expansion system; Leonard

Reiffel, et al., [redacted]/17 [IMAGE AVAILABLE]

=> d 2 kwic

US PAT NO: 5,090,026 [IMAGE AVAILABLE] L3: 2 of 8

DETDESC:

DETD(9)

The address generator 15 is illustrated in FIG. 2 as including a **serial**-to-**parallel** converter 18 using a **serial** in/**parallel** out eight-bit converter for the five most significant bits, and a interpolation counter 19 realizable as a five-stage binary counter. . . . Clock at 90.degree. reclocks Tx Data by means of the D-type flip-flop 11, clocks differential encoder 3 and clocks the **serial**-to-**parallel** interface 18. In order to generate the Tx Clock at 0.degree. the Tx Clock at 90.degree. is converted using a. . .

DETDESC:

DETD(25)

Flip-flops . . . At high resolution, the HF Reference clock signal is not divided and provided directly to line 64. The selection of **low resolution** or **high resolution** is controlled by the Select Resolution signal on line 76. With a higher frequency loop clock signal on line 64,. . .

=> d 3 kwic

US PAT NO: 5,065,346 [IMAGE AVAILABLE] L3: 3 of 8

ABSTRACT:
A **low resolution** to **high resolution** display system arranged such that a low resolution video signal from a personal computer is written in a memory plane. . .

DETDESC:

DETD(5)

The display signal derived from the V-RAM 3 is supplied to the display circuit 200, and more specifically to a **serial**-to-**parallel** converting circuit 4 and a bit clock from the display controller 1 is also supplied to the **serial**-to-**parallel** converting circuit 4, whereby parallel data is formed by the **serial**-to-**parallel** converting circuit 4 at, for example, every 16 bits. This parallel data is supplied to a memory plane 5.

=> d 4 kwic

US PAT NO: 4,949,391 [IMAGE AVAILABLE] L3: 4 of 8

DETDESC:

DETD(149)

The . . . shown in the block diagram of FIG. 9D consists of the control logic 435, the data reduction logic 440, the **serial**-in-**parallel**-out (SIPO) register 405 and the acquisition control state machine 450. The acquisition control state machine 450 runs

asynchronously t[redacted]y. . .

DETDESC:

DETD(156)

The . . . row address counter 330 (FIG. 9B) to provide the row and column addresses and support two addressing schemes which provide **low resolution** and **high resolution** image data.

DETDESC:

DETD(160)

The acquisition resolution mode (**low resolution**, uncompressed **high resolution** and compressed high resolution) is controlled by the central controller 50 (FIG. 1) by writing to the camera control register. . .

DETDESC:

DETD(161)

The . . . camera resolution mode selected, the wait time and the soak time. Table II shows maximum and minimum cycle times for **low resolution** and **high resolution** modes.

DETDESC:

DETD(162)

TABLE II

ACQUISITION CYCLE TIMES			
Low Resolution		**High Resolution**	
Min	Max	Min	Max
3.38 msec	9.86 msec	6.55 msec	13.03 msec

=> d 5 kwic

US PAT NO: 4,882,629 [IMAGE AVAILABLE] L3: 5 of 8

DETDESC:

DETD(148)

The . . . shown in the block diagram of FIG. 9D consists of the control logic 435, the data reduction logic 440, the **serial**-in-**parallel**-out (SIPO) register 405 and the acquisition control state machine 450. The acquisition control state machine 450 runs asynchronously to any. . .

DETDESC:

DETD(155)

The . . . row address counter 330 (FIG. 9B) to provide the row and column addresses and support two addressing schemes which provide **low resolution** and **high resolution** image data.

DETDESC:

DETD(159)

The acquisition resolution mode (**low resolution**, uncompressed **high resolution** and compressed high resolution) is controlled by the central controller 50 (FIG. 1) by writing to the camera control register. . .

DETDESC:

DETD(160)

The . . . camera resolution mode selected, the wait time and the soak time. Table II shows maximum and minimum cycle times for **low resolution** and **high resolution** modes.

DETDESC:

DETD(161)

TABLE II

ACQUISITION CYCLE TIMES			
Low Resolution		**High Resolution**	
Min	Max	Min	Max
3.38 msec	9.86 msec	6.55 msec	13.03 msec

=> d 6 kwic

US PAT NO: 4,851,834 [IMAGE AVAILABLE] L3: 6 of 8

ABSTRACT:
The . . . the same address location, with certain of the pixel bits removed by the mask means. The shift registers have both **serial** and **parallel** input and output means and are clocked at different speeds to accommodate different peripherals. At least a first shift register. . .

DETDESC:

DETD(37)

The . . . information can be entered into the system from peripheral devices as well as being read out of memory simultaneously by **low resolution** and **high resolution** devices, and can be repeatedly transferred between shift register units and the bit map memory to effect window scrolling presentations. . .

=> d 7 kwic

US PAT NO: 4,734,769 [IMAGE AVAILABLE] L3: 7 of 8

SUMMARY:

BSUM(9)

According . . . in a variable-intensity form. The information may be presented in a variety of formats, including: the picture only, in either

low resolution o[redacted]**gh resolution** forms, alphanum[redacted] information only [redacted] a concurrent display of both [redacted]orial and alphanumeric information. In a method which is a. . .

DETDESC:

DETD(6)

The . . . is received in serial fashion on serial data line 114. These serial representations are converted to a parallel form through **serial**-to-**parallel** converter 312. Convertor 312 produces a timing signal F on line 314 which is sent to both a clock select. . .

DETDESC:

DETD(13)

Mode . . . 326 produces a signal on line 336 when mode latch 326 is ready to cause the loading of data from **serial**-to-**parallel** convertor 312 into appropriate locations in picture memory 354. Passing the signals on lines 114 and 336 through AND gate. . .

DETDESC:

DETD(14)

In . . . is characterized by a pulse occurring each time a new set of serial data is converted to parallel form by **serial**-to-**parallel** converter 311. These pulses are sent to clock select 316, whose state causes signal J on line 327 to be. . .

DETDESC:

DETD(21)

Apparatus . . . mode until another command to receive pictorial information is received by command recognizer 320 through serial data line 114 and **serial**-to-**parallel** converter 312.

DETDESC:

DETD(22)

Referring . . . received by an RS-232 quadline receiver 500, which sends data to UART 502. Together, receiver 500 and UART 502 compose **serial**-to-**parallel** converter 312. Converter 312 produces parallel data 504, which is sent to command recognizer 320, command latch 322 and picture. . .

=> d 8 kwic

US PAT NO: 4,654,484 [IMAGE AVAILABLE] L3: 8 of 8

ABSTRACT:
An . . . which is transmitted over a narrow band communications channel. In the preferred embodiment, a video image is cyclically assembled in **low resolution** and **high resolution** phases from digitized data representing gray level intensity for individual pixels which have been grouped into pixel. During the initial. . .

SUMMARY:

BSUM(24)

This invention discloses a means for providing an image in two phases: **Low Resolution** and **High Resolution**. During the first phase, a low resolution image is generated and updated according to the results of several cycles of. . .

DETDESC:

DETD(6)

FIG. 4 is a flow diagram of the **Low Resolution** and **High Resolution** phases and the associated routines utilized in transmitting a final image from the sending station and receiving it at the. . .

DETDESC:

DETD(51)

Referring . . . analog luminance signal Y is output on line 186. The least significant bit 2.degree. passes along line 182 to a **serial** to **parallel** convertor 188.

DETDESC:

DETD(53)

Switch . . . microseconds. These switches 194, 196 alternately pass the output of the one line delay 198 or the output of the **serial** to **parallel** convertor 188. In the high state, switch 196 passes the

TRUNCATE

S#	Comment	Database	Query
S28		DWPI	lcd and low resolution video and serial to parallel conversion and analog to diigtal conversion and video signal conversion and horizontal and vertical signal synchronization
S27		DWPI	lcd and low resolution video andserial to parallel conversion
S26		DWPI	lcd andhorizontal and vertical signal synchronization andlcd and low resolution video andlow resolution video andserial to parallel conversion andanalog to diigtal conversion andvideo signal conversion
S25		DWPI	lcd andhorizontal and vertical signal synchronization
S24		DWPI	horizontal and vertical signal synchronization
S23		DWPI	video signal conversion
S22		DWPI	analog to diigtal conversion
S21		DWPI	serial to parallel conversion
S20		DWPI	low resolution video
S19		DWPI	lcd and low resolution video
S18		DWPI	lcd
S17		DWPI	convert low-resolution signal into video signal
S16		DWPI	convert low-resolution signal into video signal
S15		DWPI	display of financial information using graphic symbols: use of firm or corporate logos instead of textual obligations displayed on video wall with a plurality of monitors
S14		DWPI	display of financial information using graphic symbols: use offirm or corporate logos instead of textual obligations
S13		DWPI	display of financial information using graphic symbols
S12		DWPI	display financial information using graphic symbols
S11		DWPI	5,339,392/pn
S10		DWPI	CHOCOLATE AND CHIP AND MANUFACTURE AND MACHINE
S9		DWPI	CHOCOLATE AND CHIP AND MANUFACTURE AND MACHINE
S8		DWPI	CHOCOLATE AND CHIP AND MANUFACTURE
S7		DWPI	CHOCOLATE AND CHIP AND MANUFACTURE
S6		DWPI	CHOCOLATE CHIP MANUFACTURE
S5		DWPI	CHOCOLATE CHIP MANUFACTURE
S4		DWPI	ANTIBODY
S3		DWPI	US-5543590-$.DID.
S2		DWPI	WRIGHT-G-$.IN.
S1		DWPI	US-5729251-$.DID.

WEST 1.0

Search Queries for User d270ajb (Count = 28)

Queries 1 through 28.

Last Prev Next Goto

Help | Edit | Back | Main Menu

WEST 1.0

Help

Main Menu | Search Form | Posting Counts | Show WS Numbers | Edit WS Numbers

Search Results - Record(s) 1 through 1 of 1 returned.

der 128
der 128a
der 128b

1. Document ID: US 5646644 A DE 4023981 A DE 4023981 C2 KR 9400601 B1 US 5552801 A,

Relevance Rank: 78

Entry 1 of 1 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1991-045339

DERWENT-WEEK: 199733

TITLE:
LCD reproduces at least nine colours - uses analogue input, X-Y axis drivers and serial-parallel converter with cyclic data extraction

INVENTOR:FURUHASHI, T; FUTAMI, T ; MANO, H ; NISHIOKA, K ; TAKASHI, T

PATENT-ASSIGNEE: HITACHI LTD[HITA]

PRIORITY-DATA: 1989JP-0194094 (July 28, 1989)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 5646644 A	July 8, 1997	N/A	017	G09G 003/36
DE 4023981 A	February 7, 1991	N/A	000	N/A
DE 4023981 C2	June 24, 1993	N/A	017	G09G 003/36
KR 9400601 B1	January 26, 1994	N/A	000	G09G 003/36
US 5552801 A	September 3, 1996	N/A	018	G09G 003/36

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
US 5646644A	Cont of	1990US-0556364	July 24, 1990
US 5646644A	Cont of	1992US-0966563	October 26, 1992
US 5646644A	Cont of	1994US-0299671	September 2, 1994
US 5646644A	N/A	1996US-0646843	May 8, 1996
US 5646644A	Cont of	US 5552801	N/A
DE 4023981A	N/A	1990DE-4023981	July 27, 1990
DE 4023981C2	N/A	1990DE-4023981	July 27, 1990
KR 9400601B1	N/A	1990KR-0011154	July 23, 1990
US 5552801A	Cont of	1990US-0556364	July 24, 1990
US 5552801A	Cont of	1992US-0966563	October 26, 1992
US 5552801A	N/A	1994US-0299671	September 2, 1994

IPC: G02F001/13; G02F001/133 ; G06F003/14 ; G09G003/36

Search Results - Record(s) 1 through 14 of 14 returned.

1. Document ID: EP 298243 A ES 2088864 T3 NO 8802360 A JP 01169492 A US 4851826 A CA 1304519 C EP 298243 B1 DE 3854562 G,

Relevance Rank: 99

Entry 4 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1989-009358

DERWENT-WEEK: 199645

TITLE:
Computer video de-multiplexer for high resolution picture - has low resolution frames combined to give high resolution by stacking and reading at higher rate

INVENTOR:DAVIS, H C

PATENT-ASSIGNEE: COMMODORE ELECTRONICS LTD[COMMN], ESCOM AGE ELECTRONICS LTD[ESCON], COMMODORE ELTRN LTDCS LTD[COMMN]

PRIORITY-DATA: 1987US-0055608 (May 29, 1987)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
EP 298243 A	January 11, 1989	E	059	N/A
ES 2088864 T3	October 1, 1996	N/A	000	G09G 001/16
NO 8802360 A	December 27, 1988	N/A	000	N/A
JP 01169492 A	July 4, 1989	N/A	000	N/A
US 4851826 A	July 25, 1989	N/A	026	N/A
CA 1304519 C	June 30, 1992	N/A	000	G09G 001/16
EP 298243 B1	October 11, 1995	E	058	G09G 001/16
DE 3854562 G	November 16, 1995	N/A	000	G09G 001/16

CITED-DOCUMENTS: A3...9014; EP 148564 ; EP 92973 ; No-SR.Pub ; US 4701800 ; US 4727423

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
EP 298243A	N/A	1988EP-0108541	May 27, 1988
ES 2088864T3	N/A	1988EP-0108541	May 27, 1988
ES 2088864T3	Based on	EP 298243	N/A
JP01169492A	N/A	1988JP-0132540	May 30, 1988
US 4851826A	N/A	1987US-0055608	May 29, 1987
CA 1304519C	N/A	1988CA-0567947	May 27, 1988
EP 298243B1	N/A	1988EP-0108541	May 27, 1988
DE 3854562G	N/A	1988DE-3854562	May 27, 1988

TRUNCATE

S#	Comment	Database	Query
S28		DWPI	lcd and low resolution video and serial to parallel conversion and analog to diigtal conversion and video signal conversion and horizontal and vertical signal synchronization
S27		DWPI	lcd and low resolution video andserial to parallel conversion
S26		DWPI	lcd andhorizontal and vertical signal synchronization andlcd and low resolution video andlow resolution video andserial to parallel conversion andanalog to diigtal conversion andvideo signal conversion
S25		DWPI	lcd andhorizontal and vertical signal synchronization
S24		DWPI	horizontal and vertical signal synchronization
S23		DWPI	video signal conversion
S22		DWPI	analog to diigtal conversion
S21		DWPI	serial to parallel conversion
S20		DWPI	low resolution video
S19		DWPI	lcd and low resolution video
S18		DWPI	lcd
S17		DWPI	convert low-resolution signal into video signal
S16		DWPI	convert low-resolution signal into video signal
S15		DWPI	display of financial information using graphic symbols: use of firm or corporate logos instead of textual obligations displayed on video wall with a plurality of monitors
S14		DWPI	display of financial information using graphic symbols: use offirm or corporate logos instead of textual obligations
S13		DWPI	display of financial information using graphic symbols
S12		DWPI	display financial information using graphic symbols
S11		DWPI	5,339,392/pn
S10		DWPI	CHOCOLATE AND CHIP AND MANUFACTURE AND MACHINE
S9		DWPI	CHOCOLATE AND CHIP AND MANUFACTURE AND MACHINE
S8		DWPI	CHOCOLATE AND CHIP AND MANUFACTURE
S7		DWPI	CHOCOLATE AND CHIP AND MANUFACTURE
S6		DWPI	CHOCOLATE CHIP MANUFACTURE
S5		DWPI	CHOCOLATE CHIP MANUFACTURE
S4		DWPI	ANTIBODY
S3		DWPI	US-5543590-$.DID.
S2		DWPI	WRIGHT-G-$.IN.
S1		DWPI	US-5729251-$.DID.

Latest | Prev | Next | Oldest

Help | Edit | Back | Main Menu

WEST 1.0

Search Queries for User d270ajb (Count = 28)

Queries 1 through 28.

Latest | Prev | Next | Oldest

Help | Edit | Back | Main Menu

WEST 1.0

Help

Main Menu | Search Form | Posting Counts | Show WS Numbers | Edit WS Numbers

Search Results - Record(s) 1 through 1 of 1 returned.

der 128
der 128a
der 128b

1. Document ID: US 5646644 A DE 4023981 A DE 4023981 C2 KR 9400601 B1 US 5552801 A,

Relevance Rank: 78

Entry 1 of 1 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1991-045339

DERWENT-WEEK: 199733

TITLE:
LCD reproduces at least nine colours - uses analogue input, X-Y axis drivers and serial-parallel converter with cyclic data extraction

INVENTOR:FURUHASHI, T; FUTAMI, T ; MANO, H ; NISHIOKA, K ; TAKASHI, T

PATENT-ASSIGNEE: HITACHI LTD[HITA]

PRIORITY-DATA: 1989JP-0194094 (July 28, 1989)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 5646644 A	July 8, 1997	N/A	017	G09G 003/36
DE 4023981 A	February 7, 1991	N/A	000	N/A
DE 4023981 C2	June 24, 1993	N/A	017	G09G 003/36
KR 9400601 B1	January 26, 1994	N/A	000	G09G 003/36
US 5552801 A	September 3, 1996	N/A	018	G09G 003/36

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
US 5646644A	Cont of	1990US-0556364	July 24, 1990
US 5646644A	Cont of	1992US-0966563	October 26, 1992
US 5646644A	Cont of	1994US-0299671	September 2, 1994
US 5646644A	N/A	1996US-0646843	May 8, 1996
US 5646644A	Cont of	US 5552801	N/A
DE 4023981A	N/A	1990DE-4023981	July 27, 1990
DE 4023981C2	N/A	1990DE-4023981	July 27, 1990
KR 9400601B1	N/A	1990KR-0011154	July 23, 1990
US 5552801A	Cont of	1990US-0556364	July 24, 1990
US 5552801A	Cont of	1992US-0966563	October 26, 1992
US 5552801A	N/A	1994US-0299671	September 2, 1994

IPC: G02F001/13; G02F001/133 ; G06F003/14 ; G09G003/36

ABSTRACTED-PUB-NO:DE 4023981A
BASIC-ABSTRACT:The LCD has x-axis and y-axis drivers (112,114), an LCD screen (116) and a serial-parallel converter (110). The latter converts serial analogue image data into parallel analogue image data and can operate at high speed. The x-axis driver, which can operate at low speed, receives parallel analogue image data and delivers it for a horizontal display line of the LCD. The analogue display data are extracted cyclically from the converter using a latch clock. ADVANTAGE - Has multiple shade control and can display not fewer than nine colours using analogue input.

ABSTRACTED-PUB-NO:DE 4023981C
EQUIVALENT-ABSTRACT:The liquid-crystal display control method involves converting the digital indicating data (117R, 117G, 117B) for each pixel, which possess a breadth of several bits corresponding to the brightness, into analogue indicating data (109R, 109G, 109B) with a voltage value corresponding to the brightness involved. The D/A converter (118) is used for the conversion process. The serial analogue indicating data is converted into parallel analogue indicating data (111R, 111G, 111B) in a serial/parallel converter (110), the latter data having a lower processing speed. The voltage values are supplied by an analogue driving unit (112) for the X axis to a cell of the liquid crystal after the analogue indicating data for a horizontal line has been produced by a sequential transfer of the parallel analogue indicating data. The brightness of each pixel of the liquid-crystal screen (116) is controlled by the two converters mentioned and by the analogue driving unit. ADVANTAGE - Using analogue input signal many colours or intermediate tones can be displayed, not less than nine. A liquid crystal display device for providing signals for application to a liquid crystal display panel having a plurality of display panel rows, to cause a display made up of a plurality of display line, each display panel row of said display panel including a plurality of switching elements, each switching element normally assuming a non-selected state and responsive to application thereto of a selecting voltage for assuming a selected state, each switching element in its selected state applying to an associated display area of the display panel a voltage corresponding to data to be displayed in the associated display area and in its non-selected state retaining the associated display area at its most recent correspondi ng voltage, said liquid crystal display device comprising: a input buffer storage circuit, including a plurality m of first buffer elements, for receiving serial analog display data corresponding to a plurality of display lines and sequentially storing the received display data in said first buffer storage elements; an input holding circuit coupled to said input buffer storage circuit, for receiving and simultaneously holding the plurality of display data stored in said input buffer storage circuit; an output buffer storage circuit, including a plurality n of second buffer storage elements, where n is greater than m, for sequentially receiving said display data held in said input holding circuit and storing the received display data in the second buffer storage elements; and an output holding circuit coupled to said output buffer storage circuit, for receiving and simultaneously holding the display data stored in said output buffer storage circuit and for outputting held display data for application to switching elements of the display panel. An information processor for displaying images, said information processor comprising: (a) a display data memory circuit for storing display information for over one display image as digital data; (b) a readout circuit for successively reading out digital display image data from said display data memory circuit and for producing a timing signal synchronized with the read display data; (c) an analog display data producing circuit, including a converting circuit for successively converting the read out digital display image data to analog display data and outputting said analog display data; (d) an analog display data driving circuit including, a first holding circuit for successively receiving and holding the analog display data, a first output circuit for outputting the analog display data held by said first holding circuit, a second holding

circuit for successively receiving and holding the analog display data outputted by said first output circuit, and a second output circuit for outputting the analog display data held by said second holding circuit; (e) a Y axis direction driving circuit for outputting a selection voltage to successively select horizontal display lines in accordance with the timing signal produced by said readout circuit; and (f) a liquid crystal panel including an X axis direction driving electrode for transmitting the analog display data outputted by said analog display data driving circuit, a Y axis direction driving electrode for transmitting the selection voltage outputted by said Y axis direction driving circuit, a pixel part constituted by switching elements, pixel electrodes and liquid crystal at a location at which the X axis direction driving electrode is crossed by the Y axis direction driving electrode in a matrix state.

CHOSEN-DRAWING:Dwg.5/10 Dwg.5/10 Dwg.7,8/10 Dwg.5/10

TITLE-TERMS:
LCD REPRODUCE NINE COLOUR ANALOGUE INPUT AXIS DRIVE SERIAL PARALLEL CONVERTER CYCLIC DATA EXTRACT

DERWENT-CLASS: P81 P85 T01 T04 U14

EPI-CODES: T01-C04B; T01-C09; T04-H03B; U14-K01A3;
Non-CPI Secondary Accession Numbers:N1991-035335

Term	Documents
#110 and #15	1

Display Documents Starting At: 1

Display Format: Change Format

Search Results - Record(s) 1 through 14 of 14 returned.

1. Document ID: EP 298243 A ES 2088864 T3 NO 8802360 A JP 01169492 A US 4851826 A CA 1304519 C EP 298243 B1 DE 3854562 G,

Relevance Rank: 99

Entry 4 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1989-009358

DERWENT-WEEK: 199645

TITLE:
Computer video de-multiplexer for high resolution picture - has low resolution frames combined to give high resolution by stacking and reading at higher rate

INVENTOR:DAVIS, H C

PATENT-ASSIGNEE: COMMODORE ELECTRONICS LTD[COMMN], ESCOM AGE ELECTRONICS LTD[ESCON], COMMODORE ELTRN LTDCS LTD[COMMN]

PRIORITY-DATA: 1987US-0055608 (May 29, 1987)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
EP 298243 A	January 11, 1989	E	059	N/A
ES 2088864 T3	October 1, 1996	N/A	000	G09G 001/16
NO 8802360 A	December 27, 1988	N/A	000	N/A
JP 01169492 A	July 4, 1989	N/A	000	N/A
US 4851826 A	July 25, 1989	N/A	026	N/A
CA 1304519 C	June 30, 1992	N/A	000	G09G 001/16
EP 298243 B1	October 11, 1995	E	058	G09G 001/16
DE 3854562 G	November 16, 1995	N/A	000	G09G 001/16

CITED-DOCUMENTS: A3...9014; EP 148564 ; EP 92973 ; No-SR.Pub ; US 4701800 ; US 4727423

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
EP 298243A	N/A	1988EP-0108541	May 27, 1988
ES 2088864T3	N/A	1988EP-0108541	May 27, 1988
ES 2088864T3	Based on	EP 298243	N/A
JP01169492A	N/A	1988JP-0132540	May 30, 1988
US 4851826A	N/A	1987US-0055608	May 29, 1987
CA 1304519C	N/A	1988CA-0567947	May 27, 1988
EP 298243B1	N/A	1988EP-0108541	May 27, 1988
DE 3854562G	N/A	1988DE-3854562	May 27, 1988

DE 3854562G	N/A	1988EP-0108541	May 27, 1988
DE 3854562G	Based on	EP 298243	N/A

IPC: G06F003/15; G09G001/16 ; H04N001/38

ABSTRACTED-PUB-NO:EP 298243A
BASIC-ABSTRACT:The demultiplexer device combines several low-resolution video signals into one of high resolution. The frames from the low resolution signals are stored and read out at a higher rate, so that a number of them are combined side by side and one above the other to give one in which each of the original frames forms a part. Pref. four low-resolution frames are used with a horizontal line, of twice the original pixels, formed by corresponding original pairs of lines. Similarly the two pairs of frames placed one above the other doubles the vertical resolution. The non-data part of each transmission is used to transmit address codes so that a variety of devices can use the same input frames in different ways. USE/ADVANTAGE - Computer video output. Gives higher resolution without higher refreshing bandwidth.

ABSTRACTED-PUB-NO:EP 298243B
EQUIVALENT-ABSTRACT:A system for generating high horizontal resolution video output frames having a plurality of horizontal lines from low resolution video input frames having a plurality of horizontal lines, comprising: means (10) for receiving video input data representing a plurality of low resolution video input frames; means (16) for storing said plurality of low resolution video input frames at a first clock rate; means (18,14) for combining corresponding lines of selected ones of said plurality of stored frames to form a single horizontal line; and means (18) for outputting each said formed single horizontal line at a second clock rate substantially greater than said first clock rate thereby generating a horizontal line output having a higher resolution that the horizontal lines of said low resolution input frames. The generator comprises a device for receiving video input data representing a number of low resolution video input frames and a memory for storing the low resolution video input frames at a first clock rate. Corresp. lines of selected ones of the stored frames are combined to form a single horizontal line. Each of the formed single horizontal line is outputted at a second clock rate greater than the first clock rate thereby generating a horizontal line output having a higher resolution than the horizontal lines of the low resolution input frames. (26pp)

CHOSEN-DRAWING:Dwg.1/11 Dwg.1/11

TITLE-TERMS:
COMPUTER VIDEO DE MULTIPLEX HIGH RESOLUTION PICTURE LOW RESOLUTION FRAME COMBINATION HIGH RESOLUTION STACK READ HIGH RATE

DERWENT-CLASS: P85 T04

EPI-CODES: T04-H01A;
Non-CPI Secondary Accession Numbers:N1989-007162

Full | Citation | Review | Classification | Date | Reference

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2. Document ID: EP 629085 A2 CA 2125334 A JP 07075112 A EP 629085 A3 US 5477397 A,

Relevance Rank: 95

Entry 9 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1995-016036

DERWENT-WEEK: 199606

TITLE:
Digital high-definition television receiver facilitating trick-play modes on digital VCR - decodes received HDTV signal to produce data representing low resolution image, data representing both high and low resolution images being provided by TV receiver at output port

INVENTOR:KIM, H; NAIMPALLY, S V

PATENT-ASSIGNEE: MATSUSHITA ELEC IND CO LTD[MATU], MATSUSHITA DENKI SANGYO KK[MATU], MATSUSHITA ELEC CORP AMERICA[MATU]

PRIORITY-DATA: 1993US-0073789 (June 8, 1993) , 1993US-0021248 (February 23, 1993)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
EP 629085 A2	December 14, 1994	E	019	H04N 005/92
CA 2125334 A	December 9, 1994	N/A	000	H04N 007/12
JP 07075112 A	March 17, 1995	N/A	018	H04N 007/32
EP 629085 A3	April 12, 1995	N/A	000	H04N 005/92
US 5477397 A	December 19, 1995	N/A	017	H04N 005/78

DESIGNATED-STATES: DE FR GB NL

CITED-DOCUMENTS: No-SR.Pub; 2.Jnl.Ref ; EP 541313 ; EP 542196

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
EP 629085A2	N/A	1994EP-0108312	May 30, 1994
CA 2125334A	N/A	1994CA-2125334	June 7, 1994
JP07075112A	N/A	1994JP-0126586	June 8, 1994
EP 629085A3	N/A	1994EP-0108312	May 30, 1994
US 5477397A	CIP of	1993US-0021248	February 23, 1993
US 5477397A	N/A	1993US-0073789	June 8, 1993

IPC: H04N005/78; H04N005/92 ; H04N007/01 ; H04N007/12 ; H04N007/32

RELATED-ACC-NO: 1994-266310

ABSTRACTED-PUB-NO:EP 629085A
BASIC-ABSTRACT:The HDTV receiver comprises a receiver for the encoded high definition video signal, and a decoder (112) for decoding the video signal to produce a decoded digital signal representing the high definition video image. A decimating circuit, responsive to the decoded digital signal, decreases the number of samples in the decoded digital signal to produce a decimated video signal representing a video image having a reduced number of picture elements. An encoder encodes the decimated video signal, using intra-frame encoding techniques to the relative exclusion of predictive encoding techniques, to produce an encoded low resolution video signal. An output circuit provides both the encoded high definition video signal and the encoded low resolution video signal. The low resolution image data is also used by the TV receiver to produce a picture-in -picture (PIP) display.
ADVANTAGE - Uses single high definition television decoder to produce low resolution image data and to produce high resolution video display of television receiver.

ABSTRACTED-PUB-NO:US 5477397A
EQUIVALENT-ABSTRACT:A high-definition television receiver capable of decoding a high-definitio n video signal that was encoded using both

intra-frame and predictive encoding techniques comprising: means for receiving the encoded high-definition video signal; decoding means for decoding the encoded high-definition video signal to produce a decoded digital signal representing a high-definition video image; decimating means, responsive to the decoded digital signal, for decreasing the number of samples in the decoded digital signal to produce a decimated video signal representing a video image having a reduced number of picture elements; means for encoding the decimated video signal, using intra-frame encoding techniques to the relative exclusion of predictive encoding techniques, to produce an encoded low-resolution video signal which is independent of the encoded high-definition video signal; and output means for providing both the encoded high-definition video signal and the encoded low-resolution video signal.

CHOSEN-DRAWING:Dwg.1/10 Dwg.1/10

TITLE-TERMS:
DIGITAL HIGH DEFINE TELEVISION RECEIVE FACILITATE TRICK PLAY MODE DIGITAL VCR DECODE RECEIVE HDTV SIGNAL PRODUCE DATA REPRESENT LOW RESOLUTION IMAGE DATA REPRESENT HIGH LOW RESOLUTION IMAGE TELEVISION RECEIVE OUTPUT PORT

DERWENT-CLASS: W03 W04

EPI-CODES: W03-A11D; W03-A11X; W04-B10B; W04-B10G; W04-F01H5;
Non-CPI Secondary Accession Numbers:N1995-012665

Full | Citation | Review | Classification | Date | Reference

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3. Document ID: US 5065346 A,

Relevance Rank: 93

Entry 5 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1991-353380

DERWENT-WEEK: 199148

TITLE:
Low to high resolution display conversion system - uses buffer memory to allow low resolution video data to be simultaneously displayed in window fashion with high resolution video data

INVENTOR:KAWAI, T; TOBISHIMA, T

PATENT-ASSIGNEE: SONY CORP[SONY]

PRIORITY-DATA: 1986JP-0301051 (December 17, 1986)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 5065346 A	November 12, 1991	N/A	000	N/A

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
US 5065346A	N/A	1987US-0128069	December 3, 1987

IPC: G06F003/15; G09G001/16

ABSTRACTED-PUB-NO:US 5065346A
BASIC-ABSTRACT:The low resolution to high resolution display system is arranged such that a low resolution video signal from a personal computer is written in a memory plane in response to an address based on a clock signal produced from the personal computer side. A switching circuit is provided in a video signal path of a high resolution display appts. for switching between the memory plane and the video signal produced by the high resolution display appts. The memory plane is read by an address based on the clock signal of the display appts. produced during a display window period. The video signal read from the memory plane is supplied through the switching circuit to the video signal path of the display appts. USE - For displaying personal computer display signal on high resolution CAD/CAM appts.

CHOSEN-DRAWING:Dwg.1/3

TITLE-TERMS:
LOW HIGH RESOLUTION DISPLAY CONVERT SYSTEM BUFFER MEMORY ALLOW LOW RESOLUTION VIDEO DATA SIMULTANEOUS DISPLAY WINDOW FASHION HIGH RESOLUTION VIDEO DATA

DERWENT-CLASS: P85 T01 T04

EPI-CODES: T01-C04A; T01-J15; T04-H01;
Non-CPI Secondary Accession Numbers:N1991-270698

Full | Citation | Review | Classification | Date | Reference

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4. Document ID: JP 07107441 A,

Relevance Rank: 93

Entry 10 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1995-202642

DERWENT-WEEK: 199527

TITLE:
Video signal transmitting and receiving device - incorporates multiplexing circuit at transmission side which multiplexes data packets corresponding to compressed low resolution video signal

PATENT-ASSIGNEE: TOSHIBA KK[TOKE]

PRIORITY-DATA: 1993JP-0244867 (September 30, 1993)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 07107441 A	April 21, 1995	N/A	013	H04N 007/00

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP07107441A	N/A	1993JP-0244867	September 30, 1993

IPC: H04N007/24

ABSTRACTED-PUB-NO:JP07107441A
BASIC-ABSTRACT:The video signal transmitting and receiving device incorporates multiple encoding circuits (610-614) which encodes number of low resolution video signals. The compressed video signals from the encoding circuits is sent as data packets from multiple circuits (615-619) corresponding to N channels are multiplexed in a multiplexing circuit (620). This multiplexed video data is transmitted through a channel with high degree of resolution. In the reception side, a demultiplexing circuit (650) selects the signals for requisite channel for processing. The requisite signal is selected by recognising the header part of data packets using a decoder unit (640). ADVANTAGE - Increases freedom of selection of channels at reception side.

CHOSEN-DRAWING:Dwg.1/12

TITLE-TERMS:
VIDEO SIGNAL TRANSMIT RECEIVE DEVICE INCORPORATE MULTIPLEX CIRCUIT TRANSMISSION SIDE MULTIPLEX DATA PACKET CORRESPOND COMPRESS LOW RESOLUTION VIDEO SIGNAL

DERWENT-CLASS: W02

EPI-CODES: W02-F08; W02-K03;
Non-CPI Secondary Accession Numbers:N1995-159248

Full | Citation | Review | Classification | Date | Reference

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5. Document ID: JP 10248051 A WO 9839919 A1,

Relevance Rank: 93

Entry 13 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1998-496210

DERWENT-WEEK: 199847

TITLE:
Digital video data transmission method - separately encoding high resolution and low resolution video signals and then multiplexing encoded signals with identification information

INVENTOR:UENO, T

PATENT-ASSIGNEE: MATSUSHITA DENKI SANGYO KK[MATU], MATSUSHITA ELECTRIC IND CO LTD[MATU]

PRIORITY-DATA: 1997JP-0050154 (March 5, 1997)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 10248051 A	September 14, 1998	N/A	046	H04N 007/08
WO 9839919 A1	September 11, 1998	J	090	H04N 007/08

DESIGNATED-STATES: CA US AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP10248051A	N/A	1997JP-0050154	March 5, 1997
WO 9839919A1	N/A	1998WO-JP00906	March 5, 1998

IPC: H04N005/44; H04N007/08 ; H04N007/081 ; H04N007/24

ABSTRACTED-PUB-NO:WO 9839919A
BASIC-ABSTRACT:The digital data which is to be transmitted includes low resolution video signals (4) encoded by a low resolution compression encoder (13) and high resolution video signals (5) encoded by high resolution compression encoder (16). The two sets of encoded signals are multiplexed with a packet including identification information on a program. At the receiving side (22) the two sets of data are identified and reproduced by respective decoders (28, 30). ADVANTAGE - Increases freedom to mix video data of different resolutions, increasing flexibility of programming

CHOSEN-DRAWING:Dwg.1/34

TITLE-TERMS:
DIGITAL VIDEO DATA TRANSMISSION METHOD SEPARATE ENCODE HIGH RESOLUTION LOW RESOLUTION VIDEO SIGNAL MULTIPLEX ENCODE SIGNAL IDENTIFY INFORMATION

DERWENT-CLASS: W02 W04

EPI-CODES: W02-F07; W04-P01A;
Non-CPI Secondary Accession Numbers:N1998-387570

Full | Citation | Review | Classification | Date | Reference

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6. Document ID: US 5191416 A,

Relevance Rank: 91

Entry 6 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1993-093486

DERWENT-WEEK: 199311

TITLE:
Video signal processing system eliminating temporal aliasing - converts low-resolution video signal to format for transfer to high-resolution film and preserves realistic effect of motion from original video signal

INVENTOR:DICKSON, S P; VILLARREAL, W M

PATENT-ASSIGNEE: PACIFIC TITLE & ART STUDIO[PACIN], POST GROUP INC& ART STUDIO[POSTN]

PRIORITY-DATA: 1991US-0637486 (January 4, 1991)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 5191416 A	March 2, 1993	N/A	018	H04N 007/01

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
US 5191416A	N/A	1991US-0637486	January 4, 1991

IPC: H04N007/01; H04N007/18 ; H04N011/20

ABSTRACTED-PUB-NO:US 5191416A
BASIC-ABSTRACT:The image processing appts. converts an input video signal having a succession of interlaced fields, each representing an image at a different time, to an output video signal having a succession of non-interlaced frames. The appts. has a background generator responsive to the interlaced input video signal and providing a succession of non-interlaced background frames, each based on two or more successive associated fields on the input video signal. A motion detector senses areas of motion in the input fields corresp. to each background frame and generates data indicating the direction and magnitude of motion for each detected area. A superposition device incorporates the detected areas of motion into each background frame, to produce a succession of non-interlaced frames constituting an output video signal that preserves the effect of any motion represented in the input video signal. ADVANTAGE - Reduces signals frame rate to level compatible with that of film to be produced.

CHOSEN-DRAWING:Dwg.2/11B

TITLE-TERMS:
VIDEO SIGNAL PROCESS SYSTEM ELIMINATE TEMPORAL ALIASING CONVERT LOW RESOLUTION VIDEO SIGNAL FORMAT TRANSFER HIGH RESOLUTION FILM PRESERVE REALISTIC EFFECT MOTION ORIGINAL VIDEO SIGNAL

ADDL-INDEXING-TERMS:
CUBIC SPLINE ALGORITHM

DERWENT-CLASS: S06 W04

EPI-CODES: S06-B05; W04-D10; W04-H05; W04-N05A;
Non-CPI Secondary Accession Numbers:N1993-071585

7. Document ID: JP 06141296 A,

Relevance Rank: 91

Entry 7 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1994-204629

DERWENT-WEEK: 199425

TITLE:
Hierarchical pictorial-image coding method - has line interpolation between signal of each field which decomposes video signal into two or more signal components for improved clarity of low resolution video signals NoAbstract

PATENT-ASSIGNEE: MITSUBISHI ELECTRIC CORP[MITQ]

PRIORITY-DATA: 1992JP-0309660 (October 23, 1992)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 06141296 A	May 20, 1994	N/A	007	H04N 007/13

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP06141296A	N/A	1992JP-0309660	October 23, 1992

IPC: G06F015/66; H04N007/13 ; H04N011/04
ABSTRACTED-PUB-NO:JP06141296A
EQUIVALENT-ABSTRACT:

CHOSEN-DRAWING:Dwg.1/21

TITLE-TERMS:
HIERARCHY PICTURE IMAGE CODE METHOD LINE INTERPOLATION SIGNAL FIELD DECOMPOSE VIDEO SIGNAL TWO MORE SIGNAL COMPONENT IMPROVE CLEAR LOW RESOLUTION VIDEO SIGNAL NOABSTRACT

DERWENT-CLASS: T01 U21 W02 W04

EPI-CODES: T01-D02; T01-J10B; U21-A05A2; W02-F07; W04-P01A;
Non-CPI Secondary Accession Numbers:N1994-161293

Full | Citation | Review | Classification | Date | Reference

8. Document ID: EP 270235 A AU 8780516 A DK 8705653 A JP 63172581 A US 4875107 A US 5010419 A,

Relevance Rank: 89

Entry 1 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1988-156427

DERWENT-WEEK: 198823

TITLE:
Combined video camera and low resolution tape recording system - records low bandwidth FM signal on standard audio cassette tape and replays using rate conversion memory

INVENTOR:FANTONE, S D; HEIDT, T

PATENT-ASSIGNEE: WICKSTEAD J C[WICKI]

PRIORITY-DATA: 1986US-0938087 (December 4, 1986) , 1988US-0938087 (December 4, 1988) , 1989US-0378749 (July 23, 1989)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
EP 270235 A	June 8, 1988	E	018	N/A
AU 8780516 A	June 9, 1988	N/A	000	N/A
DK 8705653 A	June 5, 1988	N/A	000	N/A
JP 63172581 A	July 16, 1988	N/A	000	N/A
US 4875107 A	October 17, 1989	N/A	017	N/A
US 5010419 A	April 23, 1991	N/A	000	N/A

DESIGNATED-STATES: BE CH DE ES FR GB IT LI NL

CITED-DOCUMENTS: A3...9019; DE 2625154 ; DE 2900208 ; No-SR.Pub ; US 3922715 ; US 4131919 ; US 4133009 ; US 4263623 ; US 4475131 ; US 4544960 ; US 4546390

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
EP 270235A	N/A	1987EP-0309493	October 27, 1987
JP63172581A	N/A	1987JP-0282277	November 10, 1987
US 4875107A	N/A	1988US-0938087	December 4, 1988
US 5010419A	N/A	1989US-0378749	July 23, 1989

IPC: G11B020/00; H04N005/92 ; H04N007/12

ABSTRACTED-PUB-NO:EP 270235A
BASIC-ABSTRACT:The video appts. includes a camera (160) for converting light images into electrical video signals and a processor for converting the video signals into a low bandwidth frequency modulated storage signal with a bandwidth substantially lower than a standard TV video signal. A recording device (240) is provided to store the storage signal on an audio cassette, having a standard speed allowing storage of an audio bandwidth signal. The recording device has a drive for driving the cassette at higher than normal speed to increase the bandwidth storage capacity of the cassette, and a recording head for storing the storage signal on the cassette. ADVANTAGE - Highly portable and relatively low cost.

ABSTRACTED-PUB-NO:US 4875107A
EQUIVALENT-ABSTRACT:The video apparatus for storing video image on a recording medium and replaying the stored images on a display includes a camera which converts light images into electrical video signals. A processor coupled to the camera converts the electronic video signals into a low bandwidth frequency modulated storage signal with the bandwidth substantially lower than in a standard television video signal. A recorder coupled to the processor stores the low bandwidth frequency modulated storage signal on an audio cassette, which has a standard speed allowing storage of an audio bandwidth signal. The recorder includes a drive for driving the cassette at higher than normal speed to increase the bandwidth storage capacity of the cassette. The video apparatus also includes a switch mechanism for switching the video apparatus from a record mode where video images are stored on the cassette to a playback mode where the stored

images are read off the cassette and displayed on the video display. In the playback mode, the low bandwidth video signal is converted to a higher frequency standard television bandwidth video signal for display.
USE/ADVANTAGE - Camcorder. Low resolution. (17pp) The video apparatus for storing video images on a recording medium has a camera converting light images into electrical video signals. A processor coupled to the camera includes appts. for converting the electronic video signal into a low bandwidth frequency modulated analog storage signal with a bandwidth lower than a standard television video signal. A recording medium coupled to the processor stores the low bandwidth frequency modulated analog storage signal on an audio cassette having a standard speed allowing storage of an audio band-width signal. The recording incudes a driver for driving the audio cassette at higher than normal speed to increase the bandwidth storage capacity of the audio cassette and recording head for storing the low bandwidth frequency modulated analog storage signal on the audio cassette. The camera includes a lens for focusing light and an integrator for integrating the light focused by the lens and the camera inputting the electrical video signals directly to the processors. USE/ADVANTAGE - CCD based portable camcorder. Low resolution video and audio recording and playback at low cost. (14pp)

CHOSEN-DRAWING:Dwg.2/10

TITLE-TERMS:
COMBINATION VIDEO CAMERA LOW RESOLUTION TAPE RECORD SYSTEM RECORD LOW BANDWIDTH FM SIGNAL STANDARD AUDIO CASSETTE TAPE REPLAY RATE CONVERT MEMORY

DERWENT-CLASS: W04

EPI-CODES: W04-B01; W04-B10; W04-F01; W04-M01X; W04-P01C;
Non-CPI Secondary Accession Numbers:N1988-119532

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9. Document ID: EP 280932 A DE 3875983 G EP 280932 B1 JP 64000591 A US 4866520 A,

Relevance Rank: 89

Entry 2 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1988-251545

DERWENT-WEEK: 198836

TITLE:
Video signal display method for higher resolution monitor - cyclically selecting odd even and interpolated lines in preselected pattern to increase number of lines per picture

INVENTOR:MACHIDA, T; NOMURA, K ; TAKEKOSHI, T ; YAMADA, K

PATENT-ASSIGNEE: HITACHI LTD[HITA]

PRIORITY-DATA: 1987JP-0047536 (March 4, 1987)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
EP 280932 A	September 7, 1988	E	018	N/A
DE 3875983 G	December 24, 1992	N/A	000	H04N 007/01

EP 280932 B1	November 19, 1992	E	023	H04N 007/01
JP 64000591 A	January 5, 1989	N/A	000	N/A
US 4866520 A	September 12, 1989	N/A	016	N/A

DESIGNATED-STATES: DE FR GB DE FR GB

CITED-DOCUMENTS: EP 111362; GB 1525915 ; GB 1592486 ; GB 2090505 ; 01Jnl.Ref

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
EP 280932A	N/A	1988EP-0101882	February 9, 1988
DE 3875983G	N/A	1988DE-3875983	February 9, 1988
DE 3875983G	N/A	1988EP-0101882	February 9, 1988
DE 3875983G	Based on	EP 280932	N/A
EP 280932B1	N/A	1988EP-0101882	February 9, 1988
JP64000591A	N/A	1988JP-0047443	March 2, 1988
US 4866520A	N/A	1988US-0161782	February 29, 1988

IPC: G09G001/00; H04N003/22 ; H04N007/01

ABSTRACTED-PUB-NO:EP 280932A
BASIC-ABSTRACT:Each line of the lower resolution video signal is digitised to create a preselected number of digital values. Write address circuit determines appropriate memory addresses for each digital value. The addresses are indicative indicative of the line number within the picture or frame and of the position along the line. A memory (20a,20b) stores each digital value at the determined address. Read address circuit addresses are stored data in the memory at a rate controlled by the higher resolution video monitor to retrieve selected complete even and odd numbered lines of digital values. Odd line memory (20a) receives and temporarily holds each odd numbered raster line of digital values retrieved from the memory and even line memory (20b) and hold each even numbered line. An interpolating circuit (22) is connected with the even and odd line memories for interpolating the lines held. A circuit (24) cyclically selects among even, odd, and interpolated lines of data for display on the high resolution video monitor. USE/ADVANTAGE - Converts lower resolution video signals having raster lines of analog data into higher resolution video signal having larger number of raster lines. Particularly for displaying lower resolution interlaced TV signals on higher resolution CRT displays e.g. of computer monitors, without non-linear stretching of image and without line repetitions.

ABSTRACTED-PUB-NO:EP 280932B
EQUIVALENT-ABSTRACT:A method for converting an interlaced field lower resolution video signal having sequentially an odd numbers field comprising the odd-numbere d raster lines of a scanned picture in the form of analog data and an even numbers field comprising the even-numbered raster lines of a scanned picture in the form of analog data into a higher resolution video signal having sequential fields, each having a larger plurality of raster lines, the lower resolution video signal representing a picture consisting of a plurality of consecutive raster lines which are numbered consecutively, the method comprising the following steps: digitising each analog raster line of odd numbers and even numbers fields of the lower resolution video signal into a pre-selected plurality of digital values; characterised in further comprising the steps of: storing the digital values in accordance with the low resolution video signal field, line number and position within the line selectively reading digital values corresponding to adjacent raster lines in the picture; interpolating the read digital values to obtain digital values for raster lines of the higher resolution video signal; and assembling the interpolated lines and at least one of the odd numbers and even numbers field raster lines for each field of the highe The appts. comprises a A/D converter (44) assigning received lines of each even and odd line fields to given digital values. A write address circuit (56) determines a memory address m corresponding to each digital value, indicating the field, then (46) stores the digital values in conjunction

with the corresp. address. The memory is converted to the A/D converter and write address circuits. A read address circuit (72) addresses the memory to read digital values of the selected lines of the odd and even line fields. An odd line field memory (20A) and even line field memory (20B) receive and hold lines of their respective fields digital values from the buffer. An interpolator (22) takes the even and odd line digital values and produce an interpolated line. A selected (24) cyclically takes a mix of even field, odd field and interpolated lines for display in a common higher resolution field on the video monitor. USE/ADVANTAGE - Computer CRT displays, video displays. Magnifies displayed picture of video signal. Improves apparant resolution of signal. Reduced distortion, improved definition, higher quality of picture. (16pp)

CHOSEN-DRAWING:Dwg.1/12

TITLE-TERMS:
VIDEO SIGNAL DISPLAY METHOD HIGH RESOLUTION MONITOR CYCLIC SELECT ODD EVEN INTERPOLATION LINE PRESELECTED PATTERN INCREASE NUMBER LINE PER PICTURE

DERWENT-CLASS: P85 T04 W03

EPI-CODES: T04-H01; W03-A11; W03-A20;
Non-CPI Secondary Accession Numbers:N1988-191335

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10. Document ID: DE 3629462 A DE 3629462 C2 GB 2195858 A JP 63061575 A US 4825296 A CH 674269 A GB 2195858 B JP 07154727 A,

Relevance Rank: 89

Entry 3 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1988-065071

DERWENT-WEEK: 199624

TITLE:
Electronic image processing system for CRT printer - has image store in front and behind image processor with parallel store supplying display monitor

INVENTOR:FUCHSBERGE, H; RUF, W ; WAGENSONNE, E ; FUCHSBERGER, H ; WAGENSONNER, E

PATENT-ASSIGNEE: AGFA-GEVAERT AG[GEVA]

PRIORITY-DATA: 1986DE-3629462 (August 29, 1986)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
DE 3629462 A	March 3, 1988	N/A	004	N/A
DE 3629462 C2	May 15, 1996	N/A	006	H04N 001/00
GB 2195858 A	April 13, 1988	N/A	000	N/A
JP 63061575 A	March 17, 1988	N/A	000	N/A
US 4825296 A	April 25, 1989	N/A	007	N/A
CH 674269 A	May 15, 1990	N/A	000	N/A
GB 2195858 B	May 15, 1991	N/A	000	N/A
JP 07154727 A	June 16, 1995	N/A	006	H04N 005/76

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
DE 3629462A	N/A	1986DE-3629462	August 29, 1986
DE 3629462C2	N/A	1986DE-3629462	August 29, 1986
GB 2195858A	N/A	1987GB-0020315	August 28, 1987
JP63061575A	N/A	1987JP-0204312	August 19, 1987
US 4825296A	N/A	1987US-0085941	August 14, 1987
JP07154727A	Div ex	1987JP-0204312	August 19, 1987
JP07154727A	N/A	1994JP-0187025	August 19, 1987

IPC: G01T005/00; G03B027/80 ; G06F015/62 ; H04N001/00 ; H04N001/21 ; H04N005/76 ; H04N005/91

ABSTRACTED-PUB-NO:DE 3629462A
BASIC-ABSTRACT:The processing system receives the image signals obtained by electro-optic al scanning of a 2-dimensional original and supplies the corrected image signals to a CRT printer (3) for providing a positive copy. The image signal sequence is entered in a respective image store (6,7) before and after the image processor (4), with a further image store (9) for the corrected image signals coupled to a display monitor (11) for visual examination of the image. Pref. a further image processor (10) is inserted between the auxiliary image store (9) and the display monitor (11). ADVANTAGE - Increased image processing speed.

ABSTRACTED-PUB-NO:GB 2195858B
EQUIVALENT-ABSTRACT:A method of electronic image processing comprising the steps of electro-optically scanning a two-dimensional original point by point; generating raw imaging signals based on the scanning step, each pixel being accorded a respective density value; transmitting said raw signals along a predetermined path; storing said raw signals in a first part of said path; correcting the raw image signals in an image processor in a second part of said path downstream of said first part; storing the corrected signals in a third part of said path downstream of said second part; converting the corrected signals into a printable image in a fourth parth of said path downstream of said third part; and wherein each of said first part of said path is performed for an additional original, the raw signals for said additional original being stored prior to the correcting steps for said additional original at a location other than said first part of said path. An original to be copied is electrooptically scanned point-by-point. The resulting imaging signals are stored in a memory and then forwarded to an image processing unit where the signals are electronically corrected to enhance the image of the original. The corrected signals are loaded into a second memory. A portion of the corrected signals is recalled from the second memory and sent to a third memory. The portion of the corrected signals is then transmitted to a second image processing unit and converted into a low-resolution video-image which can be inspected to determine image quality. If image quality is satisfactory, the contents of the second memory are sent to an exposure unit which prints a high-resolution image of the original on copy material. Imaginq signals for a second original are loaded into the first memory as the contents of the second memory are recalled for printinq. The second processing unit functions to adjust the vide image so that it closely corresponds to the printed image of the original. (7pp)

CHOSEN-DRAWING:Dwg.1/1

TITLE-TERMS:
ELECTRONIC IMAGE PROCESS SYSTEM CRT PRINT IMAGE STORAGE FRONT IMAGE PROCESSOR PARALLEL STORAGE SUPPLY DISPLAY MONITOR

DERWENT-CLASS: P82 S06 W02 W04

EPI-CODES: S06-C02; W02-J03A; W02-J04; W04-D10;
Non-CPI Secondary Accession Numbers:N1988-049277

Full | Citation | Review | Classification | Date | Reference

11. Document ID: EP 627859 A2 EP 627859 A3 JP 07099646 A,

Relevance Rank: 89

Entry 8 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1995-008355

DERWENT-WEEK: 199502

TITLE:
Encoding and/or decoding appts for digital video signals - produces two hierarchical data signals representing e.g. conventional TV and HDTV signals

INVENTOR:FUJIMORI, Y; KAWAGUCHI, K ; KONDO, T

PATENT-ASSIGNEE: SONY CORP[SONY]

PRIORITY-DATA: 1993JP-0237431 (August 30, 1993) , 1993JP-0152836 (May 31, 1993)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
EP 627859 A2	December 7, 1994	E	018	H04N 007/13
EP 627859 A3	March 8, 1995	N/A	000	H04N 007/13
JP 07099646 A	April 11, 1995	N/A	009	H04N 007/24

DESIGNATED-STATES: DE FR GB

CITED-DOCUMENTS: No-SR.Pub; 2.Jnl.Ref ; EP 392753 ; EP 497058 ; US 4222076 ; US 5136391

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
EP 627859A2	N/A	1994EP-0303869	May 27, 1994
EP 627859A3	N/A	1994EP-0303869	May 27, 1994
JP07099646A	N/A	1993JP-0237431	August 30, 1993

IPC: G06T009/00; H04N007/13 ; H04N007/24

ABSTRACTED-PUB-NO:EP 627859A
BASIC-ABSTRACT:The apparatus produces at least two hierarchical data signals which respectively represent two (low resolution) video signals. A circuit (2) receives the input digital video signal and generates the second hierarchical data signal by calculating each pixel data signal of the second hierarchical data signal as a linear combination of N pixel data signals of the input digital video signal. A circuit (7,8) outputs the generated second hierarchical data signal together with the first hierarchical pixel data signals representing only N-1 of the N pixel data signals of the input digital video signal. Also claims a decoding apparatus. ADVANTAGE - Allows hierarchical encoding and/or decoding on digital image signal without reducing encoding efficiency and with decreased delay and hardware scale on decoding side.

CHOSEN-DRAWING:Dwg.1/9

TITLE-TERMS:
ENCODE DECODE APPARATUS DIGITAL VIDEO SIGNAL PRODUCE TWO HIERARCHY DATA SIGNAL REPRESENT CONVENTION TELEVISION HDTV SIGNAL

DERWENT-CLASS: W02 W04

EPI-CODES: W02-F06C; W04-P01A;
Non-CPI Secondary Accession Numbers:N1995-006955

Full | Citation | Review | Classification | Date | Reference

12. Document ID: US 5592299 A,

Relevance Rank: 89

Entry 11 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1997-086846

DERWENT-WEEK: 199708

TITLE:
Video image representation data reduction method - representing pair of field pictures by single field and preventing second field display by setting digital storage media byte

INVENTOR:BOYCE, J M; LANE, F A ; PEARLSTEIN, L

PATENT-ASSIGNEE: HITACHI AMERICA LTD[HITA]

PRIORITY-DATA: 1994US-0311811 (September 26, 1994)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 5592299 A	January 7, 1997	N/A	014	H04N 005/76

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
US 5592299A	N/A	1994US-0311811	September 26, 1994

IPC: H04N005/76; H04N005/78 ; H04N009/79

RELATED-ACC-NO: 1997-549150

ABSTRACTED-PUB-NO:US 5592299A
BASIC-ABSTRACT: A compressed HDTV digital video data stream is received, which includes a pair of field pictures. Both are represented by digital data. One of the field pictures of the pair is replaced by a third picture, represented by less digital data than the picture being replaced. The third picture is a transparent field. Header information associated with the pair of field pictures is generated, this being a digital storage media control byte. The byte includes a control bit set to prevent a receiver from displaying the third picture. The first and third pictures are recorded on a tape, in a tape segment from which the data can be read during the fast forward operation of a digital tape recorder. USE/ADVANTAGE - For processing digital video data to reduce amount of data required to represent a video frame. Low resolution video frames suitable for recording in trick play tape segments. No additional data needed to support trick play mode. Minimal flicker in trick play mode.

CHOSEN-DRAWING:Dwg.2/3

TITLE-TERMS:
VIDEO IMAGE REPRESENT DATA REDUCE METHOD REPRESENT PAIR FIELD PICTURE SINGLE FIELD PREVENT SECOND FIELD DISPLAY SET DIGITAL STORAGE MEDIUM BYTE

DERWENT-CLASS: W04

EPI-CODES: W04-F01;
Non-CPI Secondary Accession Numbers:N1997-071601

Full | Citation | Review | Classification | Date | Reference

13. Document ID: US 5793414 A,

Relevance Rank: 89

Entry 12 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1998-456397

DERWENT-WEEK: 199839

TITLE:
Interactive video communication system - includes printer processor which converts viewer selected relatively high resolution colour digital image to control signal for printing image on system user's dumb colour printer

INVENTOR:SHAFFER, S L

PATENT-ASSIGNEE: EASTMAN KODAK CO[EAST]

PRIORITY-DATA: 1995US-0559388 (November 15, 1995)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
US 5793414 A	August 11, 1998	N/A	007	H04N 007/16

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
US 5793414A	N/A	1995US-0559388	November 15, 1995

IPC: H04N007/14; H04N007/16

ABSTRACTED-PUB-NO:US 5793414A
BASIC-ABSTRACT:The system includes a central information facility connected to a communication channel. An interactive information database contains relatively low resolution video programming material with imbedded references to relatively high resolution colour digital images selectable by a system user. A printer processor (24) converts a viewer selected relatively high resolution colour digital image to control signals for printing the image on a system user's dumb colour printer. Multiple system users are also included, each of which is provided with a transceiver, a video display, a dumb colour printer (26) and a controller (16). The high resolution digital images referenced in the programming materials are selected by the controller. ADVANTAGE - Avoids need for dumb printer to incorporate data buffer or raster image buffer or raster image processor thereby saving expenses of such electronic units in printer. Changes system user's printer without need to reprocess images in interactive database.

CHOSEN-DRAWING:Dwg.1/3

TITLE-TERMS:
INTERACT VIDEO COMMUNICATE SYSTEM PRINT PROCESSOR CONVERT VIEW SELECT RELATIVELY HIGH RESOLUTION COLOUR DIGITAL IMAGE CONTROL SIGNAL PRINT IMAGE SYSTEM USER DUMB COLOUR PRINT

DERWENT-CLASS: W02 W04

EPI-CODES: W02-F10A; W02-F10X; W04-D10;
Non-CPI Secondary Accession Numbers:N1998-356150

Full | Citation | Review | Classification | Date | Reference

14. Document ID: JP 10222133 A,

Relevance Rank: 89

Entry 14 of 14 File:DERWENT December 8, 1998

DERWENT-ACC-NO: 1998-511109

DERWENT-WEEK: 199844

TITLE:
Drive circuit for liquid crystal display device - includes D-flip flop to divide sampling clock of frequency of 25MHz to 12.5MHz, exclusive OR gate to generate new clock signal by EX-OR divided signal with clock from timing generator

PATENT-ASSIGNEE: SONY CORP[SONY]

PRIORITY-DATA: 1997JP-0027060 (February 10, 1997)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
JP 10222133 A	August 21, 1998	N/A	009	G09G 003/36

APPLICATION-DATA:

PUB-NO	APPL-DESCRIPTOR	APPL-NO	APPL-DATE
JP10222133A	N/A	1997JP-0027060	February 10, 1997

IPC: G09G003/36; G09G005/00 ; G09G005/18 ; H04N005/66

ABSTRACTED-PUB-NO:JP10222133A
BASIC-ABSTRACT:The drive circuit includes a D-flip flop (11) which divides the sampling clock of frequency of 25MHz to a signal of frequency of 12.5MHz. The divided signal is input to an EX-OR gate (12), which EX-OR's this signal with clock from timing generator and generates a new clock signal. A video signal output unit then outputs video signal to the liquid crystal display device, synchronised with the new clock signal. ADVANTAGE - Reduces power consumption. Suppresses degradation of image quality, when low resolution video is displayed by high resolution liquid crystal display device.

CHOSEN-DRAWING:Dwg.2/11

TITLE-TERMS:
DRIVE CIRCUIT LIQUID CRYSTAL DISPLAY DEVICE FLIP DIVIDE SAMPLE CLOCK FREQUENCY EXCLUDE GATE GENERATE NEW CLOCK SIGNAL DIVIDE SIGNAL CLOCK TIME GENERATOR

DERWENT-CLASS: P85 T04 W03

EPI-CODES: T04-H03B; T04-H03C2A; W03-A08;
Non-CPI Secondary Accession Numbers:N1998-398822

Full | Citation | Review | Classification | Date | Reference

Term	Documents
low adj resolution adj video	14

Display Documents Starting At: 1

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Help

#	Patent	Source	Flag	Issue Date	Pages	Current Original Classif	Retrieval Classif	Current Cross Reference
1	5,844,538	U	U	12/01/1998	34	345/98		345/87 ...
2	5,838,292	U	U	11/17/1998	10	345/97		345/87 ...
3	5,828,367	U	U	10/27/1998	10	345/211		345/87 ...
4	5,825,341	U	U	10/20/1998	9	345/87		345/59 ...
5	5,818,411	U	U	10/06/1998	21	345/99		345/87 ...
6	5,815,134	U	U	09/29/1998	14	345/97		345/87 ...
7	5,815,131	U	U	09/29/1998	14	345/94		345/99 ...
8	5,790,090	U	U	08/04/1998	9	345/94		345/98 ...
9	5,786,800	U	U	07/28/1998	39	345/98		345/99
10	5,767,828	U	U	06/16/1998	23	345/89		345/55 ...
11	5,764,207	U	U	06/09/1998	12	345/99		345/94 ...
12	5,760,758	U	U	06/02/1998	14	345/95		345/87 ...
13	5,757,346	U	U	05/26/1998	11	345/87		345/98
14	5,757,342	U	U	05/26/1998	13	345/60		345/87 ...
15	5,754,151	U	U	05/19/1998	6	345/92		345/87 ...
16	5,751,267	U	U	05/12/1998	20	345/96		345/87 ...
17	5,748,167	U	U	05/05/1998	48	345/98		345/99
18	5,748,162	U	U	05/05/1998	12	345/87		345/94 ...
19	5,742,269	U	U	04/21/1998	9	345/87		345/94 ...
20	5,736,981	U	U	04/07/1998	58	345/507		345/87 ...
21	5,731,796	U	U	03/24/1998	75	345/96		345/87 ...
22	5,726,673	U	U	03/10/1998	10	345/87		345/94 ...
23	5,719,590	U	U	02/17/1998	19	345/94		345/99
24	5,708,454	U	U	01/13/1998	23	345/100		345/87 ...
25	5,708,453	U	U	01/13/1998	18	345/87		341/126 ...
26	5,699,076	U	U	12/16/1997	26	345/103		345/93 ...
27	5,682,176	U	U	10/28/1997	10	345/98		345/99
28	5,682,175	U	U	10/28/1997	13	345/98		345/99 ...
29	5,680,149	U	U	10/21/1997	13	345/98		345/87
30	5,675,351	U	U	10/07/1997	18	345/87		345/94 ...
31	5,668,567	U	U	09/16/1997	10	345/60		345/87 ...
32	5,657,041	U	U	08/12/1997	26	345/99		345/94
33	5,657,037	U	U	08/12/1997	20	345/94		345/78 ...
34	5,644,331	U	U	07/01/1997	11	345/99		345/98 ...
35	5,629,718	U	U	05/13/1997	8	345/99		345/94 ...
36	5,627,559	U	U	05/06/1997	9	345/97		345/87 ...
37	5,623,279	U	U	04/22/1997	25	345/98		307/404 ...
38	5,619,225	U	U	04/08/1997	34	345/98		345/88 ...
39	5,614,923	U	U	03/25/1997	10	345/99		345/95 ...
40	5,610,627	U	U	03/11/1997	34	345/99		345/87 ...
41	5,608,420	U	U	03/04/1997	18	345/89		345/94 ...
42	5,602,560	U	U	02/11/1997	13	345/94		345/58 ...
43	5,598,179	U	U	01/28/1997	21	345/98		345/94 ...
44	5,589,847	U	U	12/31/1996	23	345/98		345/87
45	5,565,884	U	U	10/15/1996	43	345/97		345/87 ...
46	5,552,801	U	U	09/03/1996	18	345/100		345/87 ...
47	5,546,102	U	U	08/13/1996	40	345/100		345/87 ...
48	5,534,884	U	U	07/09/1996	17	345/87		345/92 ...

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50	5,528,257	U	U	06/18/1996	26	345/99		345/94
51	5,519,414	U	U	05/21/1996	24	345/208		345/94 ...
52	5,515,080	U	U	05/07/1996	14	345/509		345/87 ...
53	5,489,917	U	U	02/06/1996	14	345/89		345/87 ...
54	5,483,255	U	U	01/09/1996	68	345/98		345/87
55	5,481,273	U	U	01/02/1996	11	345/94		345/87 ...
56	5,459,482	U	U	10/17/1995	22	345/98		345/87 ...
57	5,448,259	U	U	09/05/1995	12	345/99		345/98
58	5,434,589	U	U	07/18/1995	11	345/98		345/87 ...
59	5,408,226	U	U	04/18/1995	8	345/60		345/87 ...
60	5,386,217	U	U	01/31/1995	11	345/99		345/94 ...
61	5,283,564	U	U	02/01/1994	12	345/87		345/94 ...
62	5,253,091	U	U	10/12/1993	10	345/94		345/87 ...
63	5,244,596	U	U	09/14/1993	156	345/87		252/299.01 ...
64	5,243,454	U	U	09/07/1993	6	345/87		345/94
65	5,181,131	U	U	01/19/1993	6	345/87		345/97 ...
66	5,170,156	U	U	12/08/1992	32	345/85		345/87 ...
67	5,105,288	U	U	04/14/1992	9	345/87		345/94
68	5,093,736	U	U	03/03/1992	14	345/87		345/94
69	4,902,105	U	U	02/20/1990	8	345/94		345/87
70	4,754,271	U	U	06/28/1988	8	345/98		345/87 ...
71	4,748,444	U	U	05/31/1988	17	345/99		345/94 ...
72	4,743,896	U	U	05/10/1988	6	345/87		345/98
73	4,617,563	U	U	10/14/1986	7	345/87		345/98
74	4,574,282	U	U	03/04/1986	12	345/87		345/94 ...
75	4,506,955	U	U	03/26/1985	9	345/87		345/94 ...
76	4,449,125	U	U	05/15/1984	7	345/87		345/98 ...
77	4,352,102	U	U	09/28/1982	3	345/94		345/99 ...
78	4,275,421	U	U	06/23/1981	17	348/589		345/98 ...
79	4,040,719	U	U	08/09/1977	8	345/87		334/86 ...
80	4,028,692	U	U	06/07/1977	9	345/87		340/825.81 ...
81	3,861,782	U	U	01/21/1975	8	345/87		252/299.5 ...
82	3,776,615	U	U	12/04/1973	11	345/87		340/825.81 ...

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50	5,375,203	U	U	12/20/1994	11	345/511		345/515	...
51	5,369,734	U	U	11/29/1994	19	345/421		345/419	...
52	5,369,262	U	U	11/29/1994	16	345/179		235/440	...
53	5,361,081	U	U	11/01/1994	19	345/145		345/157	
54	5,355,496	U	U	10/11/1994	88	395/706		364/280	...
55	5,335,321	U	U	08/02/1994	11	345/503		345/204	
56	5,326,878	U	U	07/05/1994	6	548/315.1		548/317.1	...
57	5,317,331	U	U	05/31/1994	11	345/16		345/13	
58	5,306,726	U	U	04/26/1994	20	514/375		548/217	
59	5,300,944	U	U	04/05/1994	30	345/88		345/152	
60	5,300,926	U	U	04/05/1994	12	345/157		345/145	...
61	5,293,482	U	U	03/08/1994	12	345/517			
62	5,274,758	U	U	12/28/1993	25	345/302			
63	5,232,945	U	U	08/03/1993	18	514/456		514/374	...
64	5,227,863	U	U	07/13/1993	83	348/578		345/302	...
65	5,191,416	U	U	03/02/1993	18	348/459	PARTIAL DISPlay		
66	5,179,320	U	U	01/12/1993	12	315/399			
67	5,168,456	U	U	12/01/1992	29	364/728.03		364/726.02	
68	5,119,474	U	U	06/02/1992	25	345/302			
69	5,089,514	U	U	02/18/1992	14	514/374		514/253	...
70	5,084,392	U	U	01/28/1992	6	435/280		435/125	...
71	5,065,346	U	U	11/12/1991	7	345/428		345/115	...
72	5,051,981	U	U	09/24/1991	12	370/290		341/144	...
73	5,051,929	U	U	09/24/1991	16	345/431		345/150	...
74	5,048,077	U	U	09/10/1991	12	379/93.17		348/14	...
75	5,043,810	U	U	08/27/1991	32	348/413		348/399	
76	5,023,905	U	U	06/11/1991	13	379/93.17		340/825.4	...
77	4,972,396	U	U	11/20/1990	8	369/32		360/18	...
78	4,960,910	U	U	10/02/1990	7	549/510		544/264	...
79	4,952,951	U	U	08/28/1990	14	347/130		347/118	...
80	4,922,240	U	U	05/01/1990	23	345/100		345/205	
81	4,912,042	U	U	03/27/1990	6	435/145		435/135	...
82	4,888,795	U	U	12/19/1989	48	348/18		348/19	...
83	4,875,036	U	U	10/17/1989	7	345/104		178/18.01	...
84	4,866,520	U	U	09/12/1989	16	348/441		345/136	
85	4,839,634	U	U	06/13/1989	57	345/173		178/18.09	...
86	4,827,085	U	U	05/02/1989	31	345/174		345/104	...
87	4,825,301	U	U	04/25/1989	10	386/121		348/311	...
88	4,790,629	U	U	12/13/1988	15	345/150		84/464R	...
89	4,785,296	U	U	11/15/1988	22	345/129		345/132	...
90	4,780,760	U	U	10/25/1988	8	348/397		348/412	...
91	4,769,636	U	U	09/06/1988	26	345/340		345/342	...
92	4,751,507	U	U	06/14/1988	10	345/340		345/131	...
93	4,745,474	U	U	05/17/1988	8	348/419		375/244	
94	4,744,042	U	U	05/10/1988	27	364/726.02		968/900	...
95	4,739,414	U	U	04/19/1988	42	358/482		358/496	...
96	4,728,803	U	U	03/01/1988	47	358/465	DISPlay	358/482	...

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2	5,841,438	U	U	11/24/1998	16	345/348		345/302 ...
3	5,841,435	U	U	11/24/1998	24	345/339		345/329 ...
4	5,832,112	U	U	11/03/1998	121	382/181		382/299
5	5,819,010	U	U	10/06/1998	57	395/109		358/447 ...
6	5,812,135	U	U	09/22/1998	10	345/356		707/100
7	5,808,624	U	U	09/15/1998	66	345/435		
8	5,805,461	U	U	09/08/1998	84	364/488		364/578 ...
9	5,798,796	U	U	08/25/1998	12	348/405		348/438
10	5,798,748	U	U	08/25/1998	24	345/156		345/165 ...
11	5,754,169	U	U	05/19/1998	15	345/173		345/157 ...
12	5,751,338	U	U	05/12/1998	51	348/17		345/2 ...
13	5,729,358	U	U	03/17/1998	61	358/451		395/102
14	5,717,414	U	U	02/10/1998	12	345/8		345/7 ...
15	5,714,985	U	U	02/03/1998	22	345/508		
16	5,710,721	U	U	01/20/1998	13	395/185.04		395/183.19 ...
17	5,710,576	U	U	01/20/1998	11	345/169		345/901 ...
18	5,706,027	U	U	01/06/1998	25	345/156		73/862.043 ...
19	5,703,604	U	U	12/30/1997	23	345/8		348/36 ...
20	5,686,934	U	U	11/11/1997	18	345/97		345/99
21	5,677,708	U	U	10/14/1997	19	345/115		345/123 ...
22	5,640,543	U	U	06/17/1997	15	345/502		345/508 ...
23	5,640,131	U	U	06/17/1997	48	332/109		327/176 ...
24	5,629,696	U	U	05/13/1997	46	341/101		
25	5,629,332	U	U	05/13/1997	15	514/383		514/340 ...
26	5,611,038	U	U	03/11/1997	86	345/302		345/327 ...
27	5,604,861	U	U	02/18/1997	19	345/326		345/348 ...
28	5,597,808	U	U	01/28/1997	19	514/33		536/18.1
29	5,589,993	U	U	12/31/1996	16	386/81		348/390 ...
30	5,579,458	U	U	11/26/1996	10	345/433		345/507
31	5,579,412	U	U	11/26/1996	16	382/240		382/299
32	5,572,732	U	U	11/05/1996	84	395/701		364/280 ...
33	5,563,996	U	U	10/08/1996	35	707/521		345/341 ...
34	5,555,002	U	U	09/10/1996	13	345/121		345/127
35	5,530,457	U	U	06/25/1996	15	345/507		345/1 ...
36	5,502,419	U	U	03/26/1996	51	332/109		327/74 ...
37	5,491,789	U	U	02/13/1996	12	395/183.01		364/267 ...
38	5,488,698	U	U	01/30/1996	16	395/110		345/441 ...
39	5,477,397	U	U	12/19/1995	17	386/123		348/390 ...
40	5,459,514	U	U	10/17/1995	14	348/398		348/387 ...
41	5,438,074	U	U	08/01/1995	19	514/456		549/398
42	5,432,525	U	U	07/11/1995	33	345/2		
43	5,430,838	U	U	07/04/1995	11	345/344		345/340 ...
44	5,425,050	U	U	06/13/1995	26	375/200		380/10 ...
45	5,422,987	U	U	06/06/1995	20	345/427		345/163 ...
46	5,406,302	U	U	04/11/1995	9	345/55		340/815.41 ...
47	5,398,310	U	U	03/14/1995	24	707/541		345/341 ...
48	5,398,143	U	U	03/14/1995	8	360/48		

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2	5,798,748	U	T	08/25/1998	24	345/156		345/165 ...
(3)	5,736,981	U	T	04/07/1998	58	345/507		345/87 ...
4	5,729,358	U	T	03/17/1998	61	358/451		395/102
5	5,714,985	U	T	02/03/1998	22	345/508		
6	5,710,721	U	T	01/20/1998	13	395/185.04		395/183.19 ...
7	5,579,412	U	T	11/26/1996	16	382/240		382/299
8	5,477,397	U	T	12/19/1995	17	386/123		348/390 ...
9	5,444,834	U	T	08/22/1995	19	345/434		345/433
10	5,425,050	U	T	06/13/1995	26	375/200		380/10 ...
11	5,300,944	U	T	04/05/1994	30	345/88		345/152
12	5,293,482	U	T	03/08/1994	12	345/517		
13	5,227,863	U	T	07/13/1993	83	348/578		345/302 ...
14	5,191,416	U	T	03/02/1993	18	348/459		
15	5,065,346	U	T	11/12/1991	7	345/428		345/115 ...
16	5,051,929	U	T	09/24/1991	16	345/431		345/150 ...
17	4,888,795	U	T	12/19/1989	48	348/18		348/19 ...
18	4,866,520	U	T	09/12/1989	16	348/441		345/136
19	4,780,760	U	T	10/25/1988	8	348/397		348/412 ...
20	4,745,474	U	T	05/17/1988	8	348/419		375/244
21	4,656,468	U	T	04/07/1987	11	345/509		345/136
22	4,641,185	U	T	02/03/1987	8	358/535		358/513

Serial to Parallel Converter

=> s low resolution to high resolution

```
       1109689 LOW
        113650 RESOLUTION
       1416232 HIGH
        113650 RESOLUTION
L1         102 LOW RESOLUTION TO HIGH RESOLUTION
                 (LOW(W)RESOLUTION(1W)HIGH(W)RESOLUTION)
```

=> s serial to parallel

```
         88961 SERIAL
        856588 PARALLEL
L2       10329 SERIAL TO PARALLEL
                 (SERIAL(1W)PARALLEL)
```

=> s l1 and l2

```
L3           8 L1 AND L2
```

=> d kwic

US PAT NO: 5,481,275 [IMAGE AVAILABLE] L3: 1 of 8

DETDESC:

DETD(11)

The . . . "HR" and "HC" are used throughout to respectively represent High-resolution Row and High-resolution Column. FIG. 2 shows the relation between **low-resolution** and **high-resolution** rows and columns.

DETDESC:

DETD(36)

The . . . in FIG. 2 to show groups of four HPx's each associated with a corresponding four subposition regions, QA-QD, of each **low-resolution** pixel. **High-resolution** pixels 204 are depicted as dashed (hidden) circles in FIG. 2.

DETDESC:

DETD(128)

The . . . is that signals are repeatedly converted between parallel and serial formats as they flow downstream through a pipelined architecture. The parallel-to-**serial**-to-**parallel** conversions help to reduce the die-size and pin count of the CLIO chip 430 and help to take full advantage. . .

=> s 2 kwic

```
       2382668 2
            12 KWIC
<------User Break------>
```

u
SEARCH ENDED BY US

=>

=> d 2 kwic

US PAT NO: 5,090,026 [IMAGE AVAILABLE] L3: 2 of 8

DETDESC:

DETD(9)

The address generator 15 is illustrated in FIG. 2 as including a **serial**-to-**parallel** converter 18 using a **serial** in/**parallel** out eight-bit converter for the five most significant bits, and a interpolation counter 19 realizable as a five-stage binary counter. . . Clock at 90.degree. reclocks Tx Data by means of the D-type flip-flop 11, clocks differential encoder 3 and clocks the **serial**-to-**parallel** interface 18. In order to generate the Tx Clock at 0.degree. the Tx Clock at 90.degree. is converted using a. . .

DETDESC:

DETD(25)

Flip-flops . . . At high resolution, the HF Reference clock signal is not divided and provided directly to line 64. The selection of **low resolution** or **high resolution** is controlled by the Select Resolution signal on line 76. With a higher frequency loop clock signal on line 64,. . .

=> d 3 kwic

US PAT NO: 5,065,346 [IMAGE AVAILABLE] L3: 3 of 8

ABSTRACT:
A **low resolution** to **high resolution** display system arranged such that a low resolution video signal from a personal computer is written in a memory plane. . .

DETDESC:

DETD(5)

The display signal derived from the V-RAM 3 is supplied to the display circuit 200, and more specifically to a **serial**-to-**parallel** converting circuit 4 and a bit clock from the display controller 1 is also supplied to the **serial**-to-**parallel** converting circuit 4, whereby parallel data is formed by the **serial**-to-**parallel** converting circuit 4 at, for example, every 16 bits. This parallel data is supplied to a memory plane 5.

=> d 4 kwic

US PAT NO: 4,949,391 [IMAGE AVAILABLE] L3: 4 of 8

DETDESC:

DETD(149)

The . . . shown in the block diagram of FIG. 9D consists of the

control logic 435, the data reduction logic 440, the **serial**-in-**parallel**-out (SIPO) register 405 and the acquisition control state machine 450. The acquisition control state machine 450 runs asynchronously to any. . .

DETDESC:

DETD(156)

The . . . row address counter 330 (FIG. 9B) to provide the row and column addresses and support two addressing schemes which provide **low resolution** and **high resolution** image data.

DETDESC:

DETD(160)

The acquisition resolution mode (**low resolution**, uncompressed **high resolution** and compressed high resolution) is controlled by the central controller 50 (FIG. 1) by writing to the camera control register. . .

DETDESC:

DETD(161)

The . . . camera resolution mode selected, the wait time and the soak time. Table II shows maximum and minimum cycle times for **low resolution** and **high resolution** modes.

DETDESC:

DETD(162)

TABLE II

ACQUISITION CYCLE TIMES			
Low Resolution		**High Resolution**	
Min	Max	Min	Max
3.38 msec	9.86 msec	6.55 msec	13.03 msec

=> d 5 kwic

US PAT NO: 4,882,629 [IMAGE AVAILABLE] L3: 5 of 8

DETDESC:

DETD(148)

The . . . shown in the block diagram of FIG. 9D consists of the control logic 435, the data reduction logic 440, the **serial**-in-**parallel**-out (SIPO) register 405 and the acquisition control state machine 450. The acquisition control state machine 450 runs asynchronously to any. . .

DETDESC:

DETD(155)

The . . . row address counter 330 (FIG. 9B) to provide the row and

column addresses a[redacted] support two addressing schemes [redacted]hich provide **low resolution** and **hig[redacted]esolution** image data.

DETDESC:

DETD(159)

The acquisition resolution mode (**low resolution**, uncompressed **high resolution** and compressed high resolution) is controlled by the central controller 50 (FIG. 1) by writing to the camera control register. . .

DETDESC:

DETD(160)

The . . . camera resolution mode selected, the wait time and the soak time. Table II shows maximum and minimum cycle times for **low resolution** and **high resolution** modes.

DETDESC:

DETD(161)

TABLE II

ACQUISITION CYCLE TIMES			
Low Resolution		**High Resolution**	
Min	Max	Min	Max
3.38 msec	9.86 msec	6.55 msec	13.03 msec

=> d 1-8

1. 5,481,275, Jan. 2, 1996, Resolution enhancement for video display using multi-line interpolation; Robert J. Mical, et al., 345/132, 138, 149 [IMAGE AVAILABLE]

2. 5,090,026, Feb. 18, 1992, GMSK narrowband modem; Harold P. Stern, et al., 375/274; 329/300; 332/100; 375/296, 305, 336 [IMAGE AVAILABLE]

3. 5,065,346, Nov. 12, 1991, Method and apparatus for employing a buffer memory to allow low resolution video data to be simultaneously displayed in window fashion with high resolution video data; Toshihiko Kawai, et al., 345/428, 115, 132; 348/552 [IMAGE AVAILABLE]

4. 4,949,391, Aug. 14, 1990, Adaptive image acquisition system; James L. Faulkerson, et al., 382/313, 221 [IMAGE AVAILABLE]

5. 4,882,629, Nov. 21, 1989, Adaptive exposure control system; James L. Faulkerson, et al., 358/464, 447, 471; 382/321 [IMAGE AVAILABLE]

6. 4,851,834, Jul. 25, 1989, Multiport memory and source arrangement for pixel information; Thomas C. Stockebrand, et al., 345/509, 191, 198 [IMAGE AVAILABLE]

7. 4,734,769, Mar. 29, 1988, Method and apparatus for display of variable intensity pictures on a video display terminal; Mark A. Davis, 348/564, 461, 473, 589 [IMAGE AVAILABLE]

8. 4,654,484, Mar. 31, 1987, Video compression/expansion system; Leonard

Reiffel, et al., 3[redacted]/17 [IMAGE AVAILABLE]

=> d 2 kwic

US PAT NO: 5,090,026 [IMAGE AVAILABLE] L3: 2 of 8

DETDESC:

DETD(9)

The address generator 15 is illustrated in FIG. 2 as including a **serial**-to-**parallel** converter 18 using a **serial** in/**parallel** out eight-bit converter for the five most significant bits, and a interpolation counter 19 realizable as a five-stage binary counter. . . Clock at 90.degree. reclocks Tx Data by means of the D-type flip-flop 11, clocks differential encoder 3 and clocks the **serial**-to-**parallel** interface 18. In order to generate the Tx Clock at 0.degree. the Tx Clock at 90.degree. is converted using a. . .

DETDESC:

DETD(25)

Flip-flops . . . At high resolution, the HF Reference clock signal is not divided and provided directly to line 64. The selection of **low resolution** or **high resolution** is controlled by the Select Resolution signal on line 76. With a higher frequency loop clock signal on line 64,. . .

=> d 3 kwic

US PAT NO: 5,065,346 [IMAGE AVAILABLE] L3: 3 of 8

ABSTRACT:
A **low resolution** to **high resolution** display system arranged such that a low resolution video signal from a personal computer is written in a memory plane. . .

DETDESC:

DETD(5)

The display signal derived from the V-RAM 3 is supplied to the display circuit 200, and more specifically to a **serial**-to-**parallel** converting circuit 4 and a bit clock from the display controller 1 is also supplied to the **serial**-to-**parallel** converting circuit 4, whereby parallel data is formed by the **serial**-to-**parallel** converting circuit 4 at, for example, every 16 bits. This parallel data is supplied to a memory plane 5.

=> d 4 kwic

US PAT NO: 4,949,391 [IMAGE AVAILABLE] L3: 4 of 8

DETDESC:

DETD(149)

The . . . shown in the block diagram of FIG. 9D consists of the control logic 435, the data reduction logic 440, the **serial**-in-**parallel**-out (SIPO) register 405 and the acquisition control state machine 450. The acquisition control state machine 450 runs

asynchronously to [redacted]. . .

DETDESC:

DETD(156)

The . . . row address counter 330 (FIG. 9B) to provide the row and column addresses and support two addressing schemes which provide **low resolution** and **high resolution** image data.

DETDESC:

DETD(160)

The acquisition resolution mode (**low resolution**, uncompressed **high resolution** and compressed high resolution) is controlled by the central controller 50 (FIG. 1) by writing to the camera control register. . .

DETDESC:

DETD(161)

The . . . camera resolution mode selected, the wait time and the soak time. Table II shows maximum and minimum cycle times for **low resolution** and **high resolution** modes.

DETDESC:

DETD(162)

TABLE II

ACQUISITION CYCLE TIMES			
Low Resolution		**High Resolution**	
Min	Max	Min	Max
3.38 msec	9.86 msec	6.55 msec	13.03 msec

=> d 5 kwic

US PAT NO: 4,882,629 [IMAGE AVAILABLE] L3: 5 of 8

DETDESC:

DETD(148)

The . . . shown in the block diagram of FIG. 9D consists of the control logic 435, the data reduction logic 440, the **serial**-in-**parallel**-out (SIPO) register 405 and the acquisition control state machine 450. The acquisition control state machine 450 runs asynchronously to any. . .

DETDESC:

DETD(155)

The . . . row address counter 330 (FIG. 9B) to provide the row and column addresses and support two addressing schemes which provide **low resolution** and **high resolution** image data.

DETDESC:

DETD(159)

The acquisition resolution mode (**low resolution**, uncompressed **high resolution** and compressed high resolution) is controlled by the central controller 50 (FIG. 1) by writing to the camera control register. . .

DETDESC:

DETD(160)

The . . . camera resolution mode selected, the wait time and the soak time. Table II shows maximum and minimum cycle times for **low resolution** and **high resolution** modes.

DETDESC:

DETD(161)

TABLE II

ACQUISITION CYCLE TIMES			
Low Resolution		**High Resolution**	
Min	Max	Min	Max
3.38 msec	9.86 msec	6.55 msec	13.03 msec

=> d 6 kwic

US PAT NO: 4,851,834 [IMAGE AVAILABLE] L3: 6 of 8

ABSTRACT:
The . . . the same address location, with certain of the pixel bits removed by the mask means. The shift registers have both **serial** and **parallel** input and output means and are clocked at different speeds to accommodate different peripherals. At least a first shift register. . .

DETDESC:

DETD(37)

The . . . information can be entered into the system from peripheral devices as well as being read out of memory simultaneously by **low resolution** and **high resolution** devices, and can be repeatedly transferred between shift register units and the bit map memory to effect window scrolling presentations. . .

=> d 7 kwic

US PAT NO: 4,734,769 [IMAGE AVAILABLE] L3: 7 of 8

SUMMARY:

BSUM(9)

According . . . in a variable-intensity form. The information may be presented in a variety of formats, including: the picture only, in either

low resolution or **high resolution** forms, alphanumeric information only or concurrent display of both pictorial and alphanumeric information. In a method which is a. . .

DETDESC:

DETD(6)

The . . . is received in serial fashion on serial data line 114. These serial representations are converted to a parallel form through **serial**-to-**parallel** converter 312. Convertor 312 produces a timing signal F on line 314 which is sent to both a clock select. . .

DETDESC:

DETD(13)

Mode . . . 326 produces a signal on line 336 when mode latch 326 is ready to cause the loading of data from **serial**-to-**parallel** convertor 312 into appropriate locations in picture memory 354. Passing the signals on lines 114 and 336 through AND gate. . .

DETDESC:

DETD(14)

In . . . is characterized by a pulse occurring each time a new set of serial data is converted to parallel form by **serial**-to-**parallel** converter 311. These pulses are sent to clock select 316, whose state causes signal J on line 327 to be. . .

DETDESC:

DETD(21)

Apparatus . . . mode until another command to receive pictorial information is received by command recognizer 320 through serial data line 114 and **serial**-to-**parallel** converter 312.

DETDESC:

DETD(22)

Referring . . . received by an RS-232 quadline receiver 500, which sends data to UART 502. Together, receiver 500 and UART 502 compose **serial**-to-**parallel** converter 312. Converter 312 produces parallel data 504, which is sent to command recognizer 320, command latch 322 and picture. . .

=> d 8 kwic

US PAT NO: 4,654,484 [IMAGE AVAILABLE] L3: 8 of 8

ABSTRACT:
An . . . which is transmitted over a narrow band communications channel. In the preferred embodiment, a video image is cyclically assembled in **low resolution** and **high resolution** phases from digitized data representing gray level intensity for individual pixels which have been grouped into pixel. During the initial. . .

SUMMARY:

BSUM(24)

This invention discloses a means for providing an image in two phases: **Low Resolution** and **High Resolution**. During the first phase, a low resolution image is generated and updated according to the results of several cycles of. . .

DETDESC:

DETD(6)

FIG. 4 is a flow diagram of the **Low Resolution** and **High Resolution** phases and the associated routines utilized in transmitting a final image from the sending station and receiving it at the. . .

DETDESC:

DETD(51)

Referring . . . analog luminance signal Y is output on line 186. The least significant bit 2.degree. passes along line 182 to a **serial** to **parallel** convertor 188.

DETDESC:

DETD(53)

Switch . . . microseconds. These switches 194, 196 alternately pass the output of the one line delay 198 or the output of the **serial** to **parallel** convertor 188. In the high state, switch 196 passes the